Side-channel Attack Standard Evaluation Board

Specification

– Version 1.0 –

SASEBO

December 1, 2007

Research Center for Information Security

National Institute of Advanced Industrial Science and Technology

Index

1. Overview

The Side-channel Attack Standard Evaluation Board (SASEBO) is an FPGA board specifically designed to develop standard evaluation schemes to secure the cryptographic module against physical attacks. The basic features of SASEBO are as follows:

- ➢ 250 mm x 200 mm x 1.6 mm, FR-4, eight layers.
- ➢ Two Xilinx Virtex-II pro series FPGAs.
  - Target FPGA : XC2VP7-5FG456C for cryptographic circuits
  - Control FPGA : XC2VP30-5FG676C for board control
- ➢ 32-bit local bus between the FPGAs.
- ➢ One RS-232 port.
- ➢ 24 MHz oscillator for each FPGA.
- ➢ Two 3.3V DC power supply lines.
  - Internal regulators provide 2.5V, 1.8V, and 1.6V DC powers.
- ➢ An alternative power supply line for the target FPGA is supported to directly input 1.5–1.7V.
- ➢ Shunt resistors can be inserted to VDD and GND lines to measure the power consumptions of the FPGAs.

2. I/O Assignments

U41 Target FPGA

Signal Name	Pin Number	Input/Otput	Destination
CDA0	V17		Config
CDA1	V16		Config
CDA2	W16		Config
CDA3	Y16		Config
CDA4	Y7		Config
CDA5	W7		Config
CDA6	V7		Config
CDA7	V6		Config
BUSY	W18		Config
INIT_B	W17		Config
GCLK	W20		Config
PROG_B	B1		Config
DONE	Y18		Config
M0	Y4		SW4-1
M1	W3		SW4-2
M2	Y2		SW4-3
TCLK	B22		JTAG
TDI	D3		JTAG
TDO	D20		JTAG
TMS	A21		JTAG
PWRDWN_B	Y19		SW4-4
HSWAP_EN	A2		SW4-5
VBATT	C19		P4
DXP	C4		P5
DXN	C5		P6

Signal Name	Pin Number	Input/Output	Destination
OSCX	Y12	IN	Clock
RESETA	W8	IN	RESET
CLK	C12	IN	X1
CKK_EXT	D12	IN	CN1

Signal Name	Pin Number	Input/Output	Destination
LED0	E7	OUT	D5
LED1	C10	OUT	D6
LED2	D5	OUT	D7
LED3	F9	OUT	D8
LED4	D7	OUT	D9
LED5	B11	OUT	D10
LED6	C8	OUT	D11
LED7	C7	OUT	D12
DIPSW0	E10	IN	SW5-1
DIPSW1	D10	IN	SW5-2
DIPSW2	D11	IN	SW5-3
DIPSW3	C11	IN	SW5-4
DIPSW4	E9	IN	SW5-5
DIPSW5	F10	IN	SW5-6
DIPSW6	F11	IN	SW5-7
DIPSW7	E11	IN	SW5-8
PUSH	D9	IN	SW6

Signal Name	Pin Number	Input/Output	Destination
IOA0	L2	IO	CN7-1
IOA1	K1	IO	CN7-2
IOA2	K2	IO	CN7-3
IOA3	J1	IO	CN7-4
IOA4	J2	IO	CN7-5
IOA5	H1	IO	CN7-6
IOA6	H2	IO	CN7-7
IOA7	G1	IO	CN7-8
IOA8	G2	IO	CN7-9
IOA9	F1	IO	CN7-10
IOA10	F2	IO	CN7-11
IOA11	E1	IO	CN7-12
IOA12	E2	IO	CN7-13
IOA13	D1	IO	CN7-14
IOA14	D2	IO	CN7-15
IOA15	C1	IO	CN7-16
IOA16	C2	IO	CN7-17
IOA17	L6	IO	CN7-18
IOA18	K6	IO	CN7-19
IOA19	L3	IO	CN7-20
IOA20	K5	IO	CN7-21
IOA21	K3	IO	CN7-22
IOA22	K4	IO	CN7-23
IOA23	J3	IO	CN7-24
IOA24	H5	IO	CN7-25
IOA25	H3	IO	CN7-26
IOA26	H4	IO	CN7-27
IOA27	G3	IO	CN7-28
IOA28	G4	IO	CN7-29
IOA29	G5	IO	CN7-30
IOA30	E3	IO	CN7-31
IOA31	E4	IO	CN7-32

Signal Name	Pin Number	Input/Output	Destination
IOA32	C21	IO	CN7-33
IOA33	C22	IO	CN7-34
IOA34	D21	IO	CN7-35
IOA35	D22	IO	CN7-36
IOA36	E21	IO	CN7-37
IOA37	E22	IO	CN7-38
IOA38	F21	IO	CN7-39
IOA39	F22	IO	CN7-40
IOA40	G21	IO	CN7-41
IOA41	G22	IO	CN7-42
IOA42	H21	IO	CN7-43
IOA43	H22	IO	CN7-44
IOA44	J21	IO	CN7-45
IOA45	J22	IO	CN7-46
IOA46	K21	IO	CN7-47
IOA47	K22	IO	CN7-48
IOA48	L21	IO	CN7-49
IOA49	E19	IO	CN7-50
IOA50	E20	IO	CN7-51
IOA51	G18	IO	CN7-52
IOA52	G19	IO	CN7-53
IOA53	G20	IO	CN7-54
IOA54	H19	IO	CN7-55
IOA55	H20	IO	CN7-56
IOA56	H18	IO	CN7-57
IOA57	J20	IO	CN7-58
IOA58	K19	IO	CN7-59
IOA59	K20	IO	CN7-60
IOA60	K18	IO	CN7-61
IOA61	L20	IO	CN7-62
IOA62	K17	IO	CN7-63
IOA63	L17	IO	CN7-64

Signal Name	Pin Number	Input/Output	Destination
FPGA_DI0	P21	IN	U2
FPGA_DI1	T18	IN	Y4
FPGA_DI2	U19	IN	Y3
FPGA_DI3	U21	IN	Y2
FPGA_DI4	U22	IN	Y1
FPGA_DI5	N21	IN	T2
FPGA_DI6	N22	IN	T1
FPGA_DI7	T21	IN	W2
FPGA_DI8	T22	IN	W1
FPGA_DI9	P20	IN	V6
FPGA_DI10	M21	IN	R2
FPGA_DI11	M19	IN	R1
FPGA_DI12	N19	IN	U3
FPGA_DI13	N20	IN	V4
FPGA_DI14	P19	IN	V3
FPGA_DI15	R21	IN	V2

Signal Name	Pin Number	Input/Output	Destination
FPGA_DO0	R20	OUT	V5
FPGA_DO1	AA22	OUT	AD1
FPGA_DO2	AB21	OUT	AD2
FPGA_DO3	M20	OUT	R4
FPGA_DO4	Y21	OUT	AC2
FPGA_DO5	Y22	OUT	AC1
FPGA_DO6	R22	OUT	V1
FPGA_DO7	T20	OUT	AA5
FPGA_DO8	W21	OUT	AB2
FPGA_DO9	W22	OUT	AB1
FPGA_DO10	T19	OUT	Y5
FPGA_DO11	P22	OUT	U1
FPGA_DO12	V19	OUT	AA4
FPGA_DO13	V20	OUT	AA3
FPGA_DO14	V21	OUT	AA2
FPGA_DO15	V22	OUT	AA1

Signal Name	Pin Number	Input/Output	Destination
FPGA_A0	V3	IN	P25
FPGA_A1	AA1	IN	AE26
FPGA_A2	Y2	IN	T26
FPGA_A3	Y1	IN	AD26
FPGA_A4	W2	IN	R26
FPGA_A5	W1	IN	AC26
FPGA_A6	N2	IN	W25
FPGA_A7	P2	IN	Y25
FPGA_A8	V2	IN	AD25
FPGA_A9	V1	IN	AB26
FPGA_A10	R1	IN	W26
FPGA_A11	M2	IN	V25
FPGA_A12	U2	IN	AC25
FPGA_A13	U1	IN	AA26
FPGA_A14	P1	IN	V26
FPGA_A15	N1	IN	U26

Signal Name	Pin Number	Input/Output	Destination
FPGA_WR	T2	IN	T25
FPGA_RD	T3	IN	AB25
FPGA_RSV0	T1		Y26
FPGA_RSV1	T4		R25
FPGA_RSV2	R3		U25
FPGA_RSV3	R2		AA25

Signal Name	Pin Number	Input/Output	Destination
CPUA_TDO	N3		
CPUA_TDI	M3		
CPUA_TCK	M4		
CPUA_TMS	M5		
CPUA_HALT	M6		
CPUA_TRST	N6		

U5 Control FPGA

Signal Name	Pin Number	Input/Output	Destination
CDB0	AB21		Config
CDB1	AC21		Config
CDB2	Y20		Config
CDB3	AA20		Config
CDB4	AA7		Config
CDB5	Y7		Config
CDB6	AC6		Config
CDB7	AB6		Config
BUSY	AB22		Config
INIT_B	AC22		Config
GCLK	AE24		Config
PROG_B	B1		Config
DONE	AD23		Config
M0	AE3		SW8-1
M1	AF3		SW8-2
M2	AD4		SW8-3
TCLK	B26		JTAG
TDI	D3		JTAG
TDO	D24		JTAG
TMS	B24		JTAG
PWRDWN_B	AF24		SW8-4
HSWAP_EN	B3		SW8-5
VBATT	A24		P13
DXP	A3		P14
DXN	C4		P15

Signal Name	Pin Number	Input/Output	Destination
OSCX	AE1	OUT	Clock
RESETB	Y9	IN	RESET
CLK	B13	IN	X2

Signal Name	Pin Number	Input/Output	Destination
LED0	C17	OUT	D15
LED1	B19	OUT	D16
LED2	D17	OUT	D17
LED3	A19	OUT	D18
LED4	C20	OUT	D19
LED5	D18	OUT	D20
LED6	E17	OUT	D21
LED7	C18	OUT	D22
DIPSW0	E21	IN	SW9-1
DIPSW1	D20	IN	SW9-2
DIPSW2	E19	IN	SW9-3
DIPSW3	D15	IN	SW9-4
DIPSW4	C15	IN	SW9-5
DIPSW5	B14	IN	SW9-6
DIPSW6	E15	IN	SW9-7
DIPSW7	E16	IN	SW9-8
PUSH	E22	IN	SW10

Signal Name	Pin Number	Input/Output	Destination
TX	M25	OUT	RS-232
RX	M26	IN	RS-232
CTS	N25	OUT	RS-232
RTS	L26	IN	RS-232

Signal Name	Pin Number	Input/Output	Destination
IOB0	N3	IO	CN11-1
IOB1	M4	IO	CN11-2
IOB2	L3	IO	CN11-3
IOB3	K3	IO	CN11-4
IOB4	K4	IO	CN11-5
IOB5	G3	IO	CN11-6
IOB6	G4	IO	CN11-7
IOB7	F3	IO	CN11-8
IOB8	F4	IO	CN11-9
IOB9	E4	IO	CN11-10
IOB10	N2	IO	CN11-11
IOB11	M1	IO	CN11-12
IOB12	M2	IO	CN11-13
IOB13	L1	IO	CN11-14
IOB14	L2	IO	CN11-15
IOB15	K1	IO	CN11-16
IOB16	K2	IO	CN11-17
IOB17	J1	IO	CN11-18
IOB18	J2	IO	CN11-19
IOB19	H1	IO	CN11-20
IOB20	H2	IO	CN11-21
IOB21	G1	IO	CN11-22
IOB22	G2	IO	CN11-23
IOB23	F1	IO	CN11-24
IOB24	F2	IO	CN11-25
IOB25	E1	IO	CN11-26
IOB26	E2	IO	CN11-27
IOB27	D1	IO	CN11-28
IOB28	D2	IO	CN11-29
IOB29	C1	IO	CN11-30
IOB30	C2	IO	CN11-31
IOB31	E23	IO	CN11-32

Signal Name	Pin Number	Input/Output	Destination
IOB32	F23	IO	CN11-33
IOB33	F24	IO	CN11-34
IOB34	G23	IO	CN11-35
IOB35	G24	IO	CN11-36
IOB36	H22	IO	CN11-37
IOB37	J21	IO	CN11-38
IOB38	J22	IO	CN11-39
IOB39	K23	IO	CN11-40
IOB40	J24	IO	CN11-41
IOB41	L22	IO	CN11-42
IOB42	K24	IO	CN11-43
IOB43	M23	IO	CN11-44
IOB44	M22	IO	CN11-45
IOB45	N24	IO	CN11-46
IOB46	N23	IO	CN11-47
IOB47	C25	IO	CN11-48
IOB48	C26	IO	CN11-49
IOB49	D25	IO	CN11-50
IOB50	D26	IO	CN11-51
IOB51	E25	IO	CN11-52
IOB52	E26	IO	CN11-53
IOB53	F25	IO	CN11-54
IOB54	F26	IO	CN11-55
IOB55	G25	IO	CN11-56
IOB56	G26	IO	CN11-57
IOB57	H25	IO	CN11-58
IOB58	H26	IO	CN11-59
IOB59	J25	IO	CN11-60
IOB60	J26	IO	CN11-61
IOB61	K25	IO	CN11-62
IOB62	K26	IO	CN11-63
IOB63	L25	IO	CN11-64

Signal Name	Pin Number	Input/Output	Destination
FPGA_DI0	U2	OUT	P21
FPGA_DI1	Y4	OUT	T18
FPGA_DI2	Y3	OUT	U19
FPGA_DI3	Y2	OUT	U21
FPGA_DI4	Y1	OUT	U22
FPGA_DI5	T2	OUT	N21
FPGA_DI6	T1	OUT	N22
FPGA_DI7	W2	OUT	T21
FPGA_DI8	W1	OUT	T22
FPGA_DI9	V6	OUT	P20
FPGA_DI10	R2	OUT	M21
FPGA_DI11	R1	OUT	M19
FPGA_DI12	U3	OUT	N19
FPGA_DI13	V4	OUT	N20
FPGA_DI14	V3	OUT	P19
FPGA_DI15	V2	OUT	R21

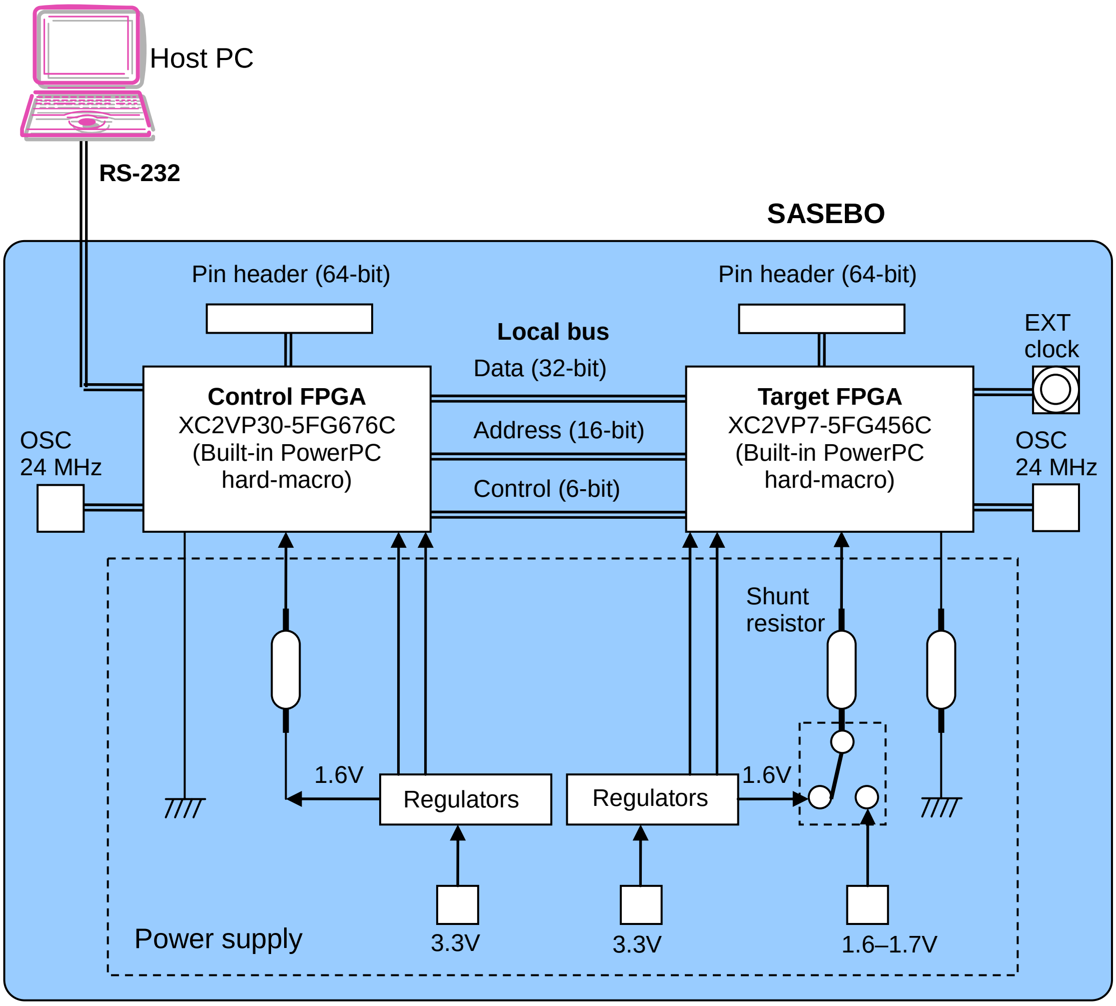
Signal Name	Pin Number	Input/Output	Destination
FPGA_DO0	V5	IN	R20
FPGA_DO1	AD1	IN	AA22
FPGA_DO2	AD2	IN	AB21
FPGA_DO3	R4	IN	M20
FPGA_DO4	AC2	IN	Y21
FPGA_DO5	AC1	IN	Y22
FPGA_DO6	V1	IN	R22
FPGA_DO7	AA5	IN	T20
FPGA_DO8	AB2	IN	W21
FPGA_DO9	AB1	IN	W22
FPGA_DO10	Y5	IN	T19
FPGA_DO11	U1	IN	P22
FPGA_DO12	AA4	IN	V19
FPGA_DO13	AA3	IN	V20
FPGA_DO14	AA2	IN	V21
FPGA_DO15	AA1	IN	V22

Signal Name	Pin Number	Input/Output	Destination
FPGA_A0	P25	OUT	V3
FPGA_A1	AE26	OUT	AA1
FPGA_A2	T26	OUT	Y2
FPGA_A3	AD26	OUT	Y1
FPGA_A4	R26	OUT	W2
FPGA_A5	AC26	OUT	W1
FPGA_A6	W25	OUT	N2
FPGA_A7	Y25	OUT	P2
FPGA_A8	AD25	OUT	V2
FPGA_A9	AB26	OUT	V1
FPGA_A10	W26	OUT	R1
FPGA_A11	V25	OUT	M2
FPGA_A12	AC25	OUT	U2
FPGA_A13	AA26	OUT	U1
FPGA_A14	V26	OUT	P1
FPGA_A15	U26	OUT	N1

Signal Name	Pin Number	Input/Output	Destination
FPGA_WR	T25	OUT	T2
FPGA_RD	AB25	OUT	T3
FPGA_RSV0	Y26		T1
FPGA_RSV1	R25		T4
FPGA_RSV2	U25		R3
FPGA_RSV3	AA25		R2

Signal Name	Pin Number	Input/Output	Destination
CPUB_TDO	R23		
CPUB_TDI	P23		
CPUB_TCK	P22		
CPUB_TMS	P24		
CPUB_HALT	P21		
CPUB_TRST	R22		

3. Block Diagram



4. Operational Instructions

4.1. Board Setting

4.1.1. Power supply

The 3.3V DC power is supplied from the connecters CN2 and CN4.

CN2: Target FPGA power supply

CN4: Control FPGA power supply

Pin assignments for the connecters CN2 and CN4 are given below.

CN2, CN4	Pin 1: DC 3.3V
	Pin 2: GND
	Pin 3: NC

DC 1.5-1.7V power can be supplied to the target FPGA directly from connecter CN5 without using the voltage regulators on the board. **Configuration switch SW3 must be set properly.** (See Section 4.1.2)
The pin assignment of CN5 is given below.

CN5 Pin 1: DC 1.5-1.7V
Pin 2: GND
Pin 3: NC

After supplying power sources to the connecters CN2 and CN4, turn on the main power switch SW1. Then the LEDs D1 and D3 indicate the status of power supplied to the target FPGA and control FPGA as follows.

D1: Power is supplied to the target FPGA.
D3: Power is supplied to the control FPGA.

4.1.2. Setting of power source for the target device

The power source for the target FPGA can be selected from the internal regulator and the external power supply (CN5) by setting SW3 as follows.

SW3 INT: The internal regulator is used.
EXT: An external power supply connected to CN5 is used.

NOTE: **Do not toggle SW3** while power is supplied to the board.

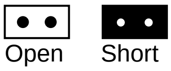
4.1.3. Setting of power sequence for the FPGA I/O

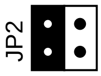
The power sequence of the target FPGA and control FPGA are configured using jumper pins JP4, JP7, and JP2.

JP4: Set the target FPGA power sequence.
Open: Power is supplied from CN2 when the voltage becomes stable. (default)
Short: Power sequence control is disabled and power is supplied directly from CN2.

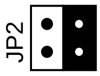
JP7: Set the control FPGA power sequence.
Open: Power supplied from CN4 is controlled by the JP2 setting. (default)
Short: The power sequence control of CN4 is disabled. The power is supplied directly.

JP2: Set CN4 power sequence





Power is supplied from CN4 when the output voltage of the 2.5V regulator becomes stable. (default)

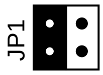


Power is supplied from CN4 when the output voltage of the 1.5V regulator becomes stable.

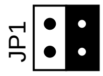
4.1.4. Setting for the FPGA configuration sequence

The configuration sequence for each FPGA is controlled using JP1 and JP6.

JP1: Setting of the configuration sequence for the target FPGA.

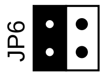


FPGA configuration starts when the output voltage of the 2.5V regulator becomes stable. (default)

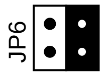


FPGA configuration starts when the output voltage of the 1.5V regulator becomes stable.

JP6: Setting of the configuration sequence for the control FPGA.



FPGA configuration starts when the output voltage of the 2.5V regulator becomes stable. (default)



FPGA configuration starts when the output voltage of the 1.5V regulator becomes stable.

4.1.5. Setting of the bypass jumper of the shunt resistors

Shunt resistors are mounted to measure the power consumed by the FPGAs as voltage drop, but they can be bypassed using jumpers JP3, JP8, and JP10 as follows.

JP3: Setting for shunt resistor R2 inserted to the 1.5V VDD line of the target FPGA core.
JP8: Setting for shunt resistor R114 inserted to the GND line of the target FPGA.
JP10: Setting for shunt resistor R125 inserted to the 1.5V VDD line of the control FPGA core.
Open: Shunt resistor is enabled. (default)
Short: Shunt resistor is bypassed.

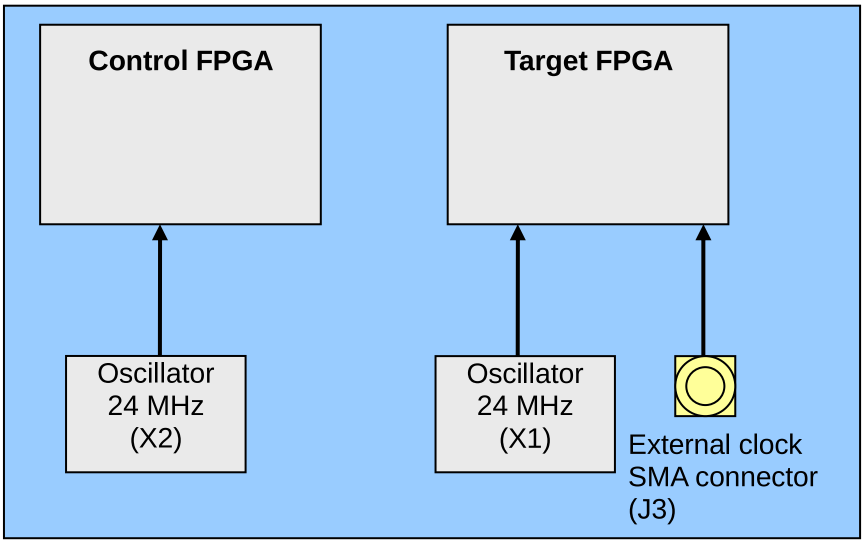
NOTE: **Keep JP5 and JP11 OPEN for the default setting.** The board will be seriously damaged if JP5 or JP11 is shorted.

4.2. Clock Sources

Two 24-MHz oscillators are implemented for the FPGAs, and the system clocks can be monitored at TP26, J4, and TP15.

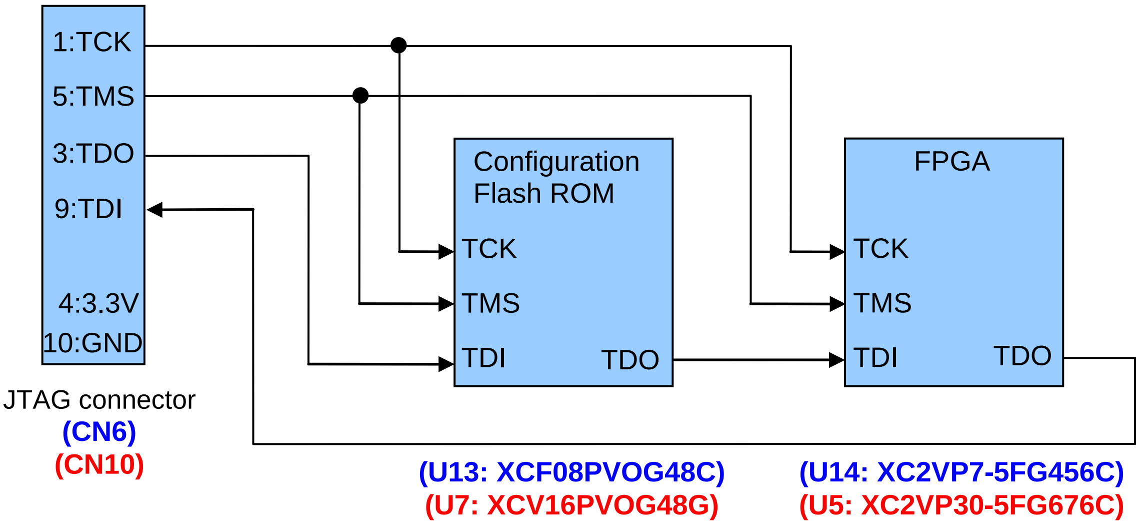
TP26, J4:	The 24 MHz clock for the control FPGA.
TP15:	The 24 MHz clock for the target FPGA.

An external clock for the target FPGA can also be supplied from J3 (SMA connector) for the target FPGA, and the clock is monitored at TP2.



4.3. FPGA Configuration

The figure below shows the connections of the FPGA, a configuration flash ROM, and a JTAG connector.



The pin assignments for CN6 (for the target FPGA) and CN10 (for the control FPGA) are as follows:

CN6, CN10:	Pin 1: TCK	Pin 2: GND
	Pin 3: TDO	Pin 4: 3.3V
	Pin 5: TMS	Pin 6: NC
	Pin 7: NC	Pin 8: NC
	Pin 9: TCI	Pin 10: GND

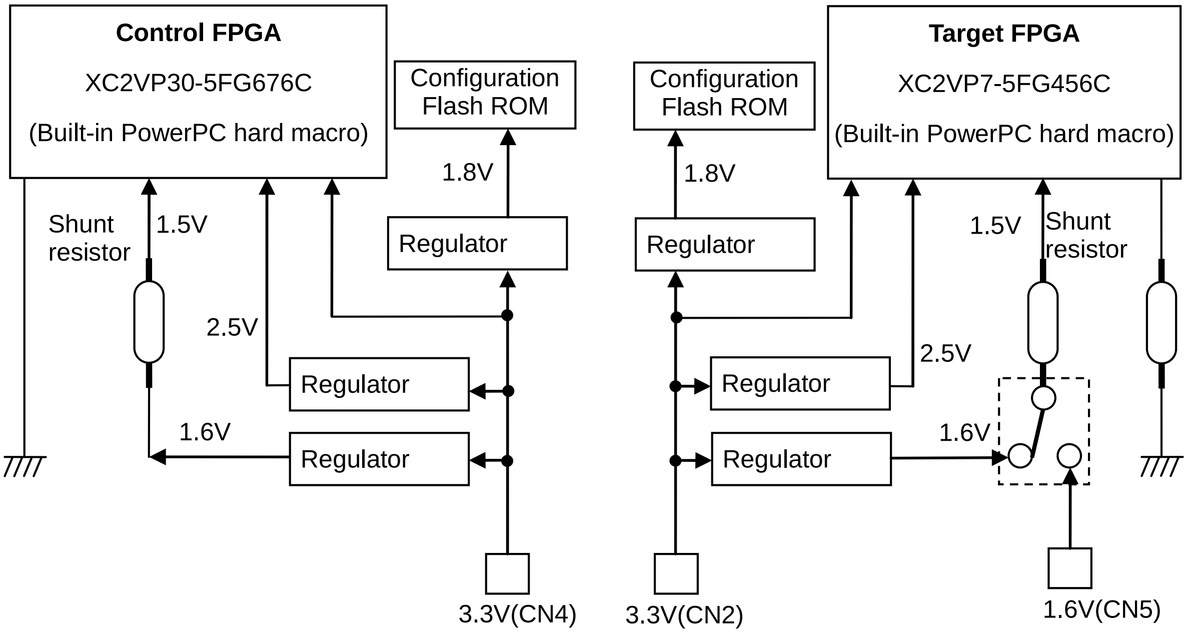
LEDs D4 and D14 are turned on when the target FPGA and control FPGA, respectively, are configured successfully. Configuration mode is set using SW4 and SW8 for the target and control FPGAs, respectively. The default configuration mode is the Master SelectMap Mode. The pin assignments of SW4 and SW8 are follows:

SW4, SW8:	1: M0	(default: off)
	2: M1	(default: off)
	3: M2	(default: on)
	4: PWRDWN	(default: off)
	5: HSWAP	(default: off)
	6-8: NC	

When configuration switch SW2 or SW7 is pushed, the configuration of the target or control FPGA, respectively, is restarted.

4.4. Power Supply

The FPGA bard receives 3.3V DC power through connectors CN2 and CN4, and then the internal power regulators generate three voltages of 2.5V, 1.8V, and 1.6V. Alternatively, the 1.6V power for the target FPGA core can be provided from connector CN5.



The pin assignments of connectors CN2, CN4, and CN5 for the 3.3V power supplies and test points TP1 and TP11 for the voltage monitor are described below.

CN2: Power supply to the target FPGA.
1: VCC
2: GND
3: NC
TP1: Test pin to monitor the CN2 voltage.

CN4: Power supply to the control FPGA.

1: VCC

2: GND

3: NC

TP11: Test pin to monitor the CN4 voltage.

Internal 2.5V regulator（TPS72625DCQ）

TP12: Test pin to monitor the 2.5V power supply for the target FPGA.

TP23: Test pin to monitor the 2.5V power supply for the control FPGA.

Internal 1.8V regulator（PQ1U181M2ZPH）

TP14: Test pin to monitor the 1.8V power supply for the configuration flash ROM dedicated to the target FPGA.

TP25: Test pin to monitor the 1.8V power supply for the configuration flash ROM dedicated to the control FPGA.

Internal 1.6V regulator（MAX8556ETE）

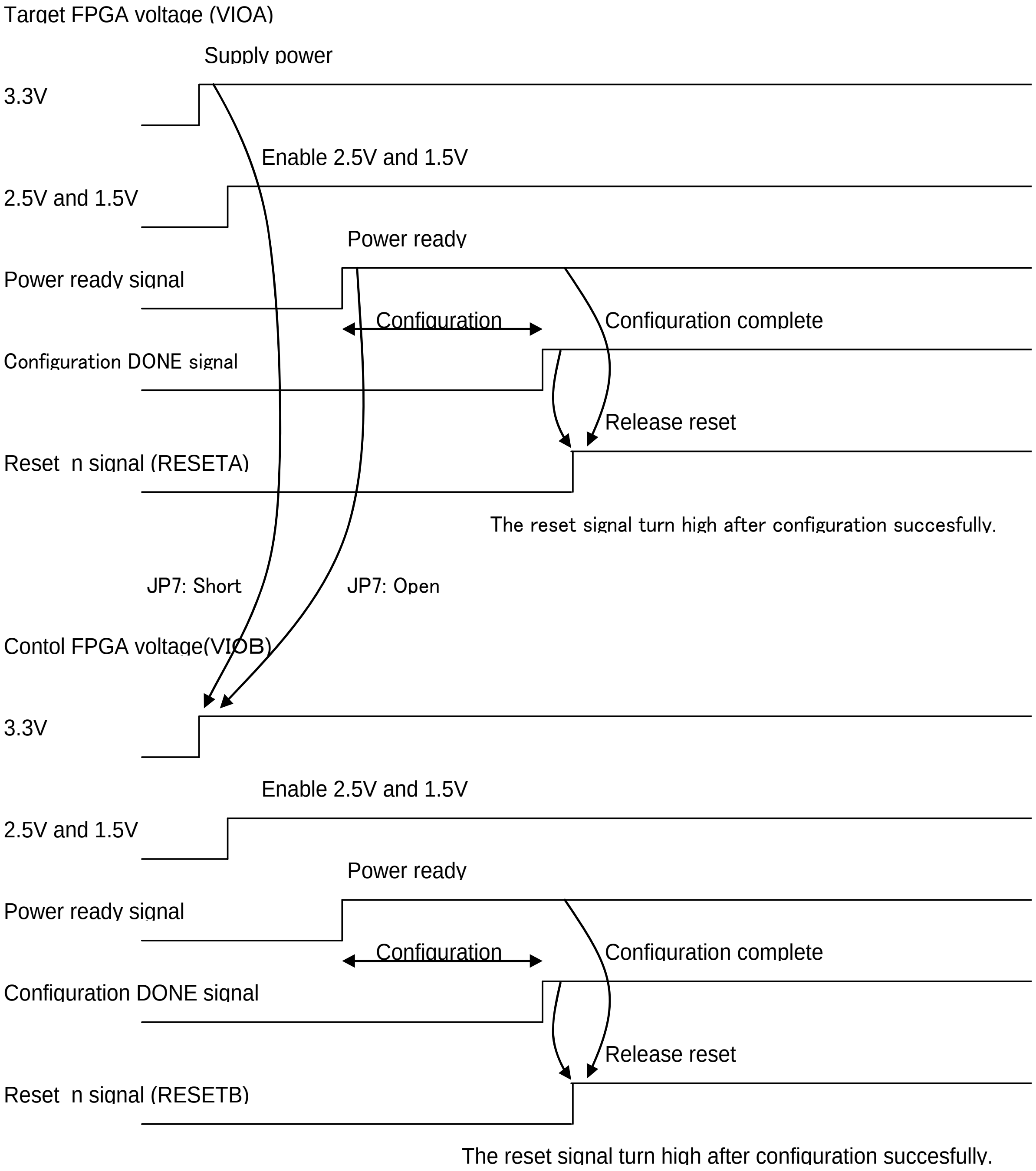
CN5: Direct power supply for the target FPGA core.

1: VCC

2: GND

3: NC

TP3: Test pin to monitor the 1.6V power supply for the target FPGA core.



4.5. Serial Interface

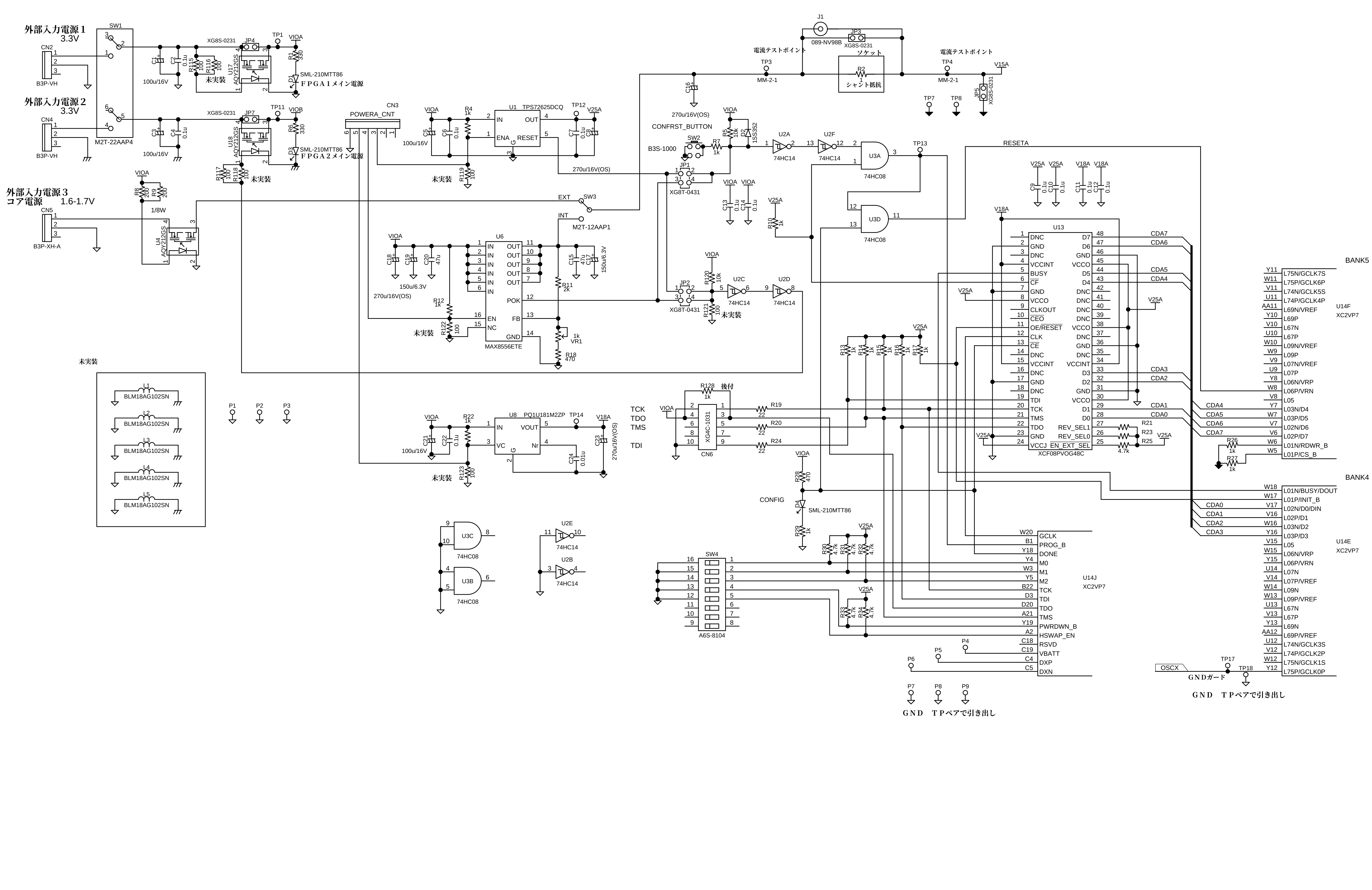
Use a female-female 9-pin-9-pin RS-232 straight cable to connect the RS-232C port (XM2C-0912-111: OMRON D-Sub male connector) to a host PC.

Signal Name	**CN12 （XM2C-0912-111）**	**U16 (ADM3202ARN)**		**U5 (XC2VP30-5FG676C)**
TX	2pin	14pin	11pin	M25
RX	3pin	13pin	12pin	M26
CTS	8pin	7pin	10pin	N25
RTS	7pin	8pin	9pin	L26

5. Board Schematic

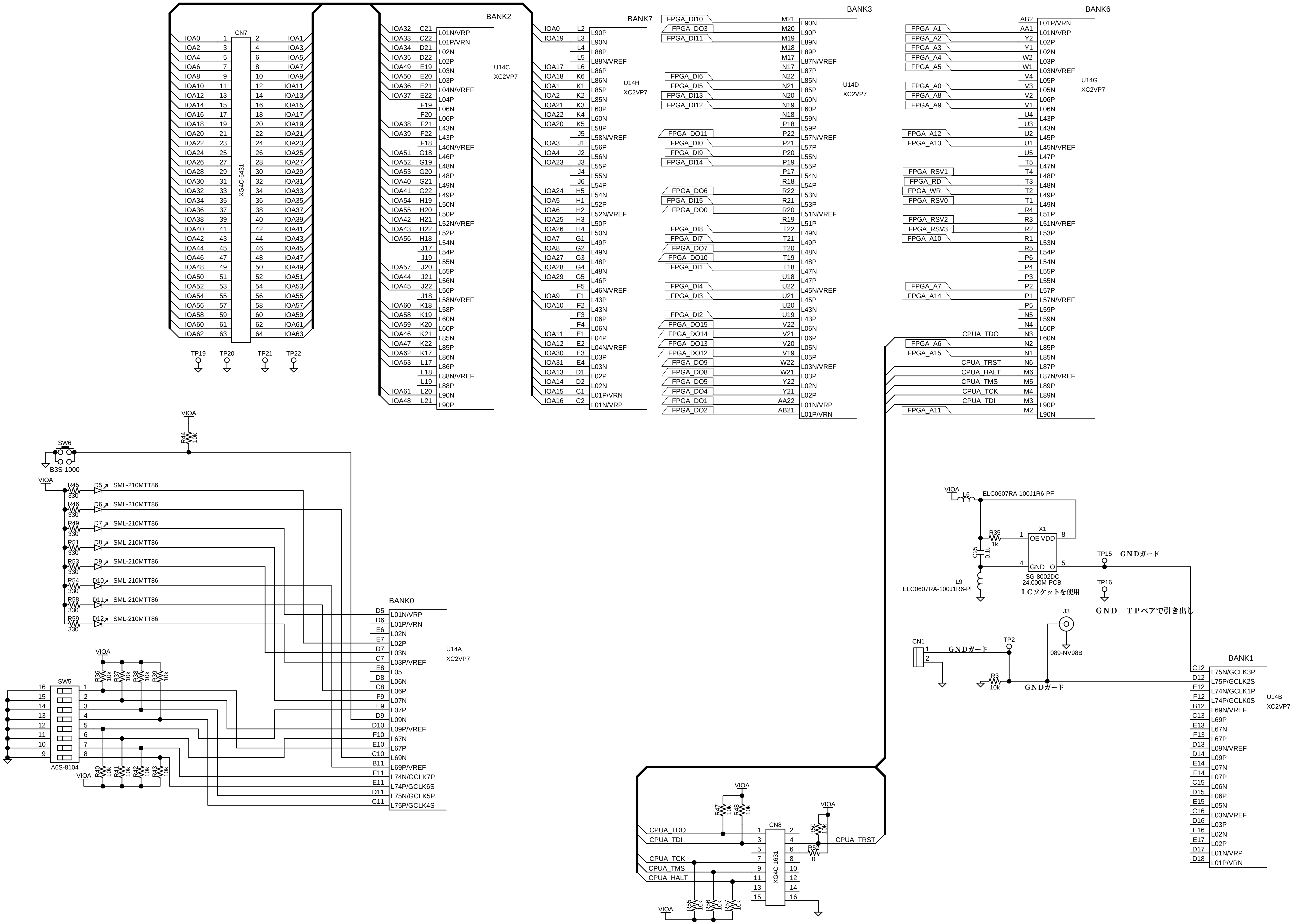
【Target Device Block】

【Control Device Block】



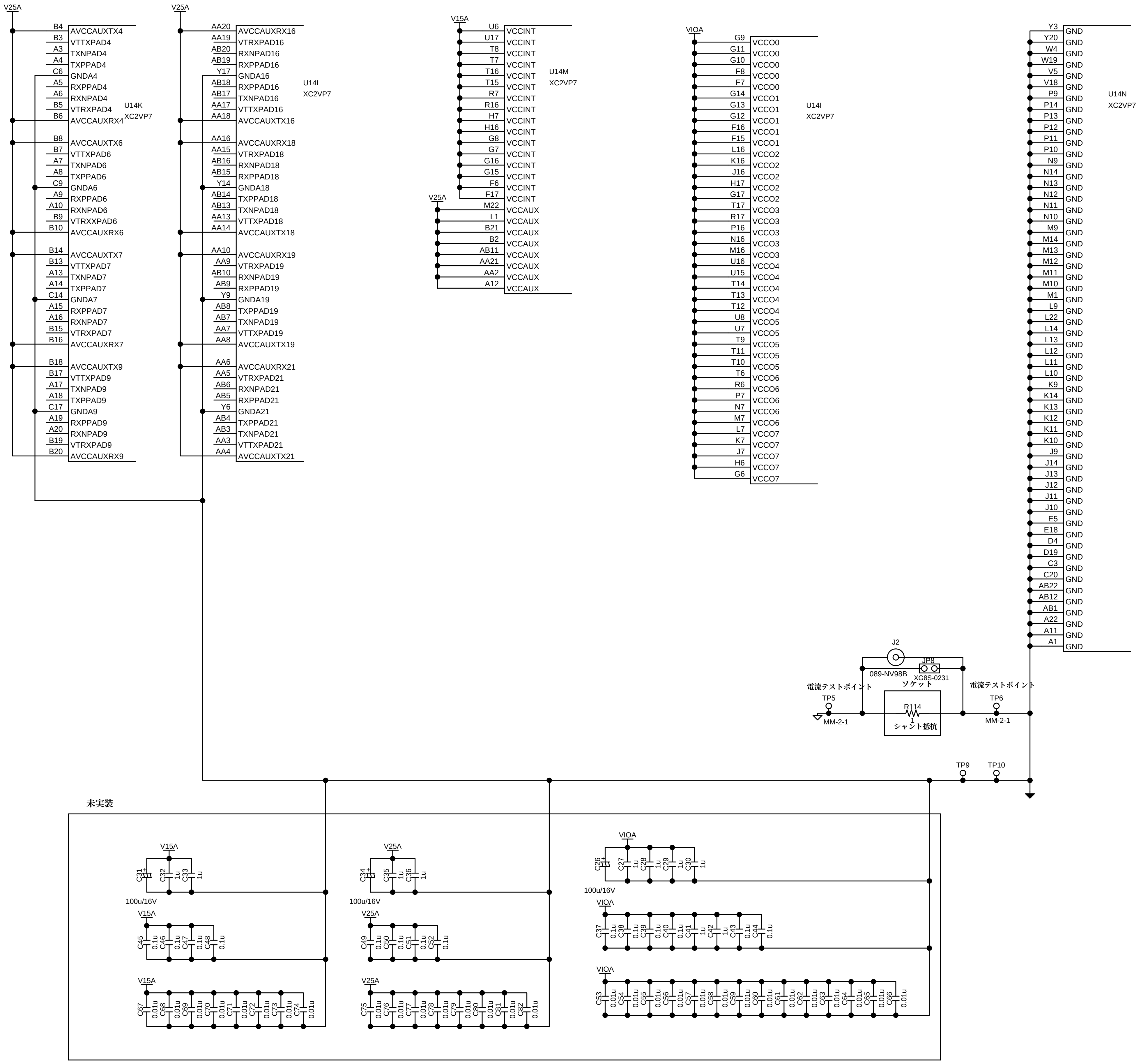
TITLE	DRAWING_No.
	E3-93961-1

SHEET	DATE	DESIGN
1 ／ 6		



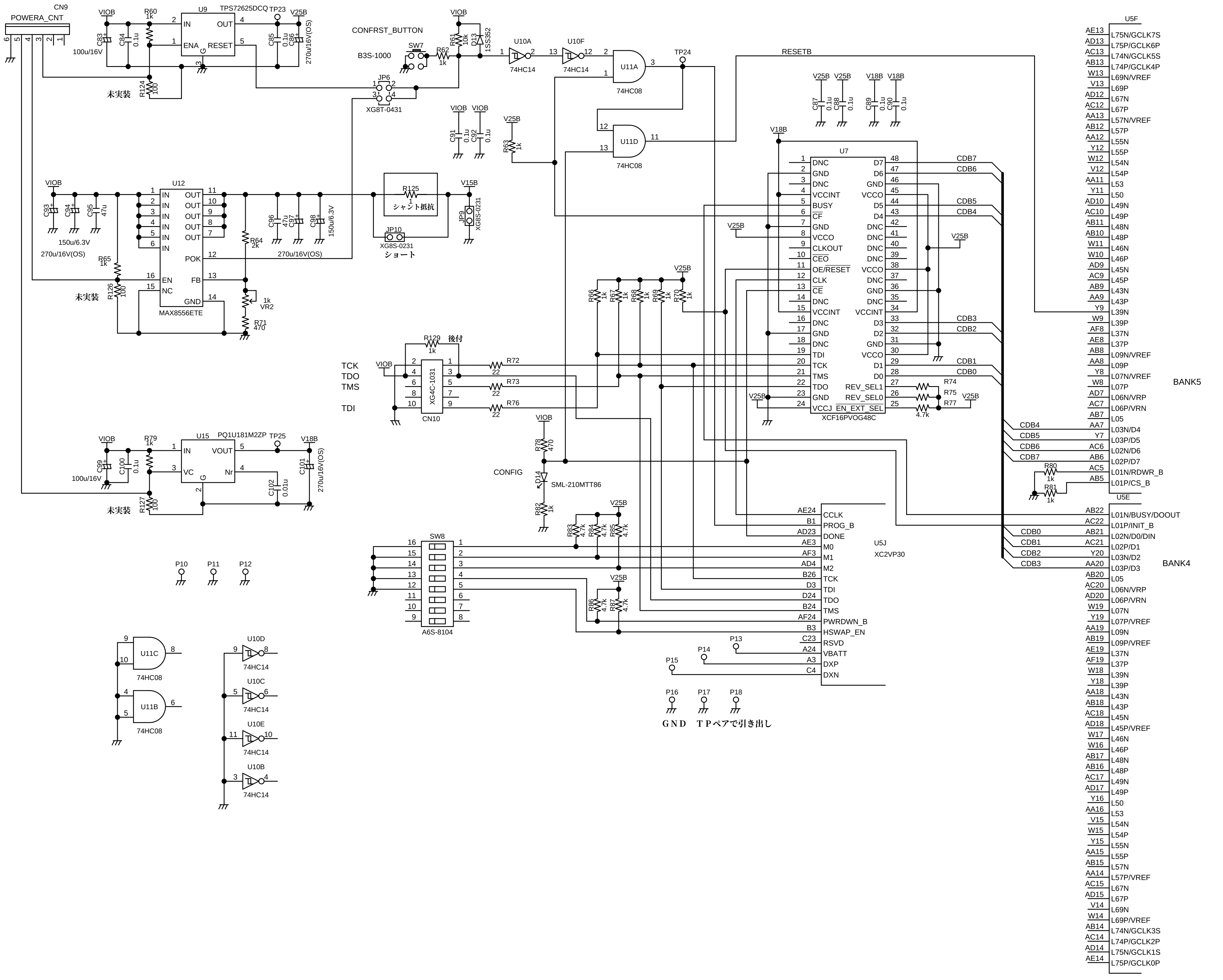
TITLE	DRAWING_No.
	E3-93961-1

SHEET	DATE	DESIGN
2 ／ 6		



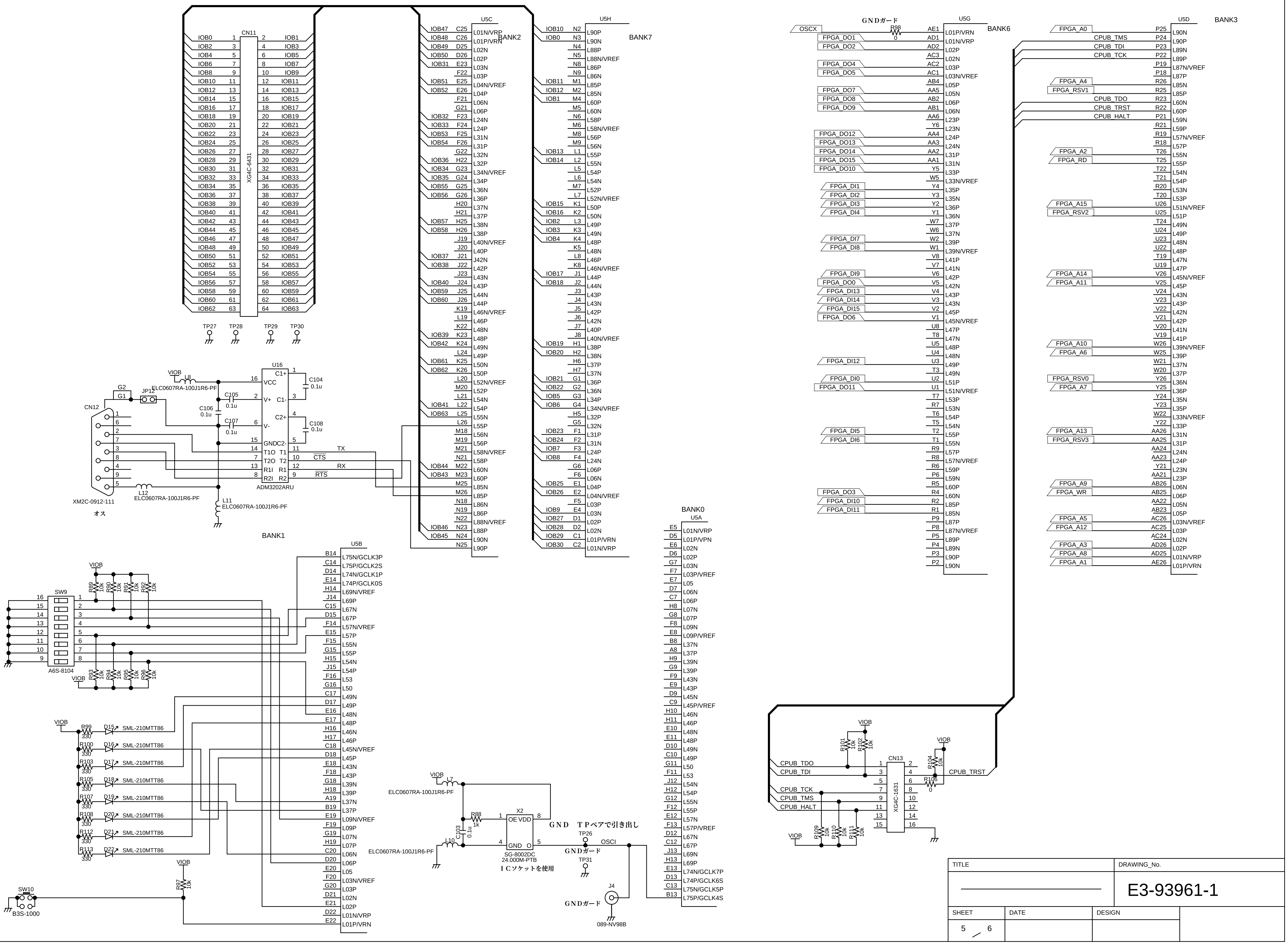
TITLE		DRAWING_No.
		E3-93961-1

SHEET	DATE	DESIGN	
3 ／ 6			



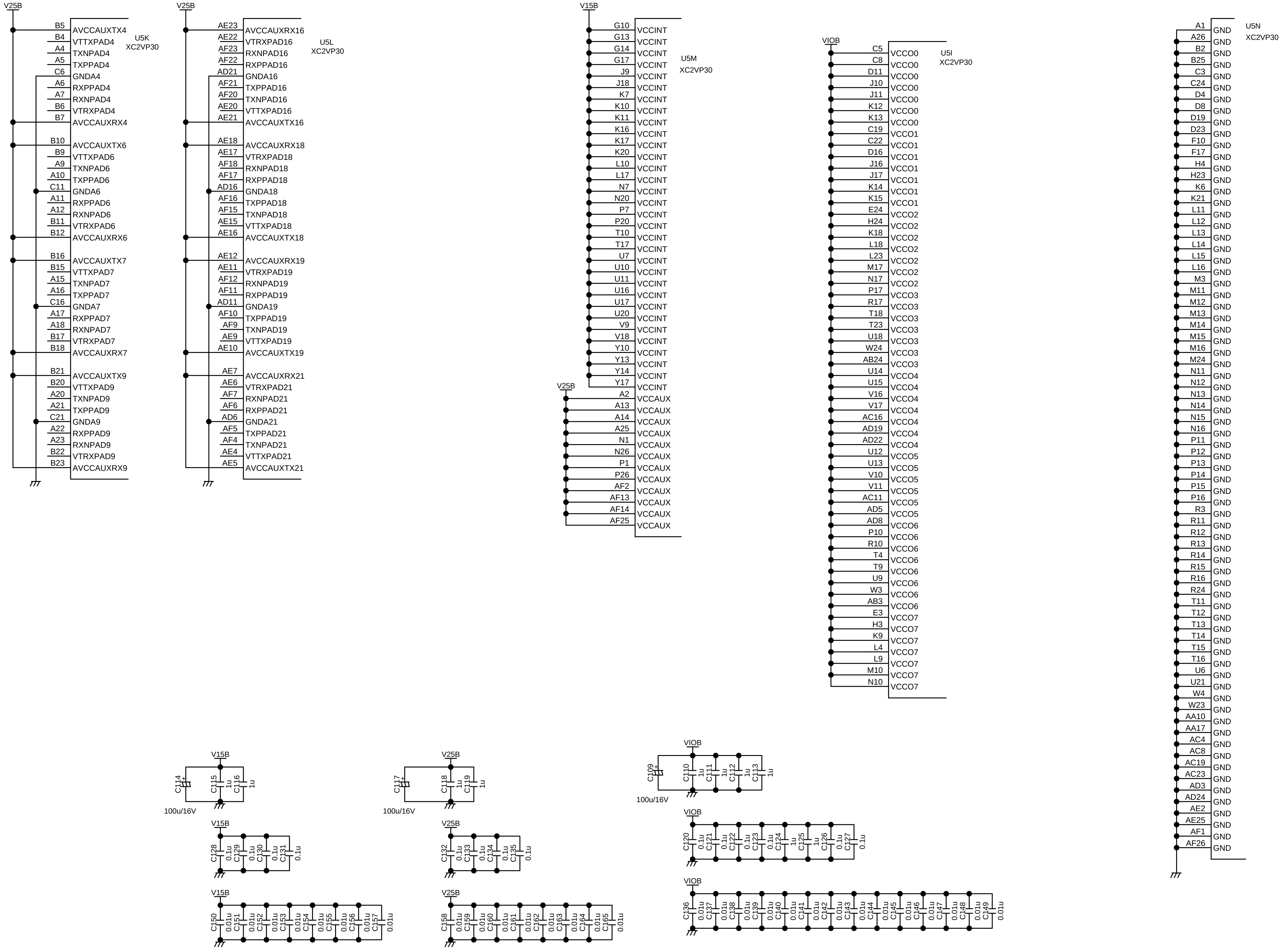
TITLE	DRAWING_No.
	E3-93961-1

SHEET	DATE	DESIGN
4 ／ 6		



TITLE	DRAWING_No.
	E3-93961-1

SHEET	DATE	DESIGN
5 ／ 6		



TITLE	DRAWING_No.
	E3-93961-1

SHEET	DATE	DESIGN	
6 / 6			

6. Part List

Board Name	Side-channel Attack Standard Evaluation Board
Model Number	3-93296-1

Type	Model	Manufacture	Qty	Components
Capacitor	GRM155F11H103ZA57E	MURATA	32	C24,C53,C54,C55,C56,C57,C58,C59,C60,C61 C62,C63,C64,C65,C66,C67,C68,C69,C70,C71 C72,C73,C74,C75,C76,C77,C78,C79,C80,C81 C82,C102,C136,C137,C138,C139,C140,C141 C142,C143,C144,C145,C146,C147,C148,C149 C150,C151,C152,C153,C154,C155,C156,C157 C158,C159,C160,C161,C162,C163,C164,C165
Capacitor	GRM155F11E104ZA01D	MURATA	41	C2,C4,C6,C7,C9,C10,C11,C12,C13,C14,C22 C25,C37,C38,C39,C40,C43,C44,C45,C46,C47 C48,C49,C50,C51,C52,C84,C85,C87,C88,C89 C90,C91,C92,C100,C103,C104,C105,C106 C107,C108,C120,C121,C122,C123,C126,C127 C128,C129,C130,C131,C132,C133,C134,C135
Capacitor	GRM155F11E105ZE01D	MURATA	10	C27,C28,C29,C30,C32,C33,C35,C36,C41,C42 C110,C111,C112,C113,C115,C116,C118,C119 C124,C125
Capacitor	C4532JF1C476Z	TDK	4	C15,C20,C95,C96 (4532 47u/16V)
Capacitor	EMV-6R3ADA101MF55G	Nippon Chemi-Con	9	C1,C3,C5,C21,C26,C31,C34,C83,C99,C109 C114,C117 (100u/6.3V)
Capacitor	EEFUE0J151R	Panasonic	4	C17,C19,C94,C98 (150u/6.3V)
Capacitor	APSA100ELL271MHB5S	Nippon Chemi-Con	8	C8,C16,C18,C23,C86,C93,C97,C101
Diode	1SS352(-TPH3)	TOSHIBA	2	D2,D13
Inductor	BLM18BD182SN1D	MURATA	5	L1,L2,L3,L4,L5
Inductor	ELC0607RA-100J1R6-PF	TDK	7	L6,L7,L8,L9,L10,L11,L12 (ELC0607S-100J1R6-PF)
Connector	DF1-2P-2.5DSA	HIROSE	1	CN1
Connector	DF1-6P-2.5DSA	HIROSE	2	CN3,CN9
Regulator	PQ1U181M2ZPH	SHARP	2	U8,U15
Regulator	TPS72625DCQ	TI	2	U1,U9
Regulator	MAX8556ETE	MAX	2	U6,U12
FPGA	XC2VP30-5FG676C	Xilinx	1	U5
FPGA	XC2VP7-5FG456C	Xilinx	1	U14
ROM	XCF08PVOG48C	Xilinx	1	U13
ROM	XCF16PVOG48C	Xilinx	1	U7
CMOS	SN74HC08NS	TI	2	U3,U11
CMOS	SN74HC14NSE4	TI	2	U2,U10
RS-232 level shifter	ADM3202ARUZ	Analog device	1	U16
LED	SML-210MTT86	ROHM	20	D1,D3,D4,D5,D6,D7,D8,D9,D10,D11,D12 D14,D15,D16,D17,D18,D19,D20,D21,D22
Connector	XG4C-1031	OMRON	2	CN6,CN10
Connector	XG4C-1631	OMRON	2	CN8,CN13
Jumper	XG8T-0431	OMRON	3	JP1,JP2,JP6
Jumper	XG8S-0231	OMRON	7	JP3,JP4,JP5,JP7,JP8,JP9,JP10
GU Photo MOS	AQY212GS	Panasonic	3	U4,U17,U18
SG-8002DC	24.000M-PCB	Epson	2	X1,X2
Resistor	RK73Z1JTD 0Ω	KOA	3	R52,R98,R106
Resistor	RR0816P-103-D	SSM	32	R3,R5,R36,R37,R38,R39,R40,R41,R42,R43 R47,R48,R50,R55,R56,R57,R61,R89,R90,R91

				R92,R93,R94,R95,R96,R101,R102,R104 R109,R110,R111,R120
Resistor	RR0816P-102-D	SSM	30	R4,R7,R10,R12,R13,R14,R15,R16,R17,R22 R26,R27,R28,R29,R35,R60,R62,R63,R65,R66 R67,R68,R69,R70,R79,R80,R81,R82,R88,R128 R129
Resistor	RR0816P-201-D	SSM	2	R8,R9
Resistor	RR0816P-220-D	SSM	6	R19,R20,R24,R72,R73,R76
Resistor	RR0816P-331-D	SSM	18	R1,R6,R45,R46,R49,R51,R53,R54,R58,R59 R99,R100,R103,R105,R107,R108,R112,R113
Resistor	RR0816P-472-D	SSM	18	R21,R23,R25,R30,R31,R32,R33,R34,R44,R74 R75,R77,R83,R84,R85,R86,R87,R97
Resistor	RR0816P-471-D	SSM	4	R18,R28,R71,R78
Resistor	RR0816P-202-D	SSM	2	R11,R64
Resistor	RR0816P-101-D	SSM	2	R115,R116,R117,R118,R119,R120,R121,R122 R123,R124,R126,R127
Trimmer	ST-32EA 1KΩ(13)	COPAL	2	VR1,VR2
Socket	089-NV98B	YUETSU SEIKI	4	J1,J2,J3,J4
Socket	XM2C-0912-111	OMRON	1	CN12
Connector	A1-64PA-2.54DSA(71)	HIROSE	2	CN7,CN11
Connector	B3P-VH(LF)(SN)	JST	2	CN2,CN4
Connector	B3B-XH-A(LF)(SN)	JST	1	CN5
Resistor	ERX1SJ1R0	Panasonic	3	R2,R114,R125
Switch	A6S-8104	OMRON	4	SW4,SW5,SW8,SW9
Switch	B3S-1000	OMRON	4	SW2,SW6,SW7,SW10
Switch	CS-12AAP1	Nikkai	1	SW3
Switch	CS-22AAP1	Nikkai	1	SW1
Test point	LC-3-G(yellow)	MAC8	12	TP1,TP2,TP11,TP12,TP13,TP14,TP15,TP17 TP23,TP24,TP25,TP26
Test point	LC-3-G(black)	MAC8	15	TP7,TP8,TP9,TP10,TP16,TP18,TP19,TP20 TP21,TP22,TP27,TP28,TP29,TP30,TP31
Test point	MM-2-1	MAC8	4	TP3,TP4,TP5,TP6
Jumper socket	XJ8A-0211	OMRON	10	
Socket	R110-91-308	PRECI-DIP	2	
Socket	PM-3	MAC8	1	
Socket	VHR-3N	JST	2	CN2,CN4
Socket	BVH-41T-P1.1	JST	4	CN2,CN4
Rubber	BU-692-A	SATO PARTS	4	
Spacer	ASB320	HIROSUGI-KEIKI	4	
Screw	M3×8		4	
Screw	M3×6		4	
Connector	XG4H-1031	OMRON	2	JTAG exchanger
Connector	87832-1420	MOLEX	2	JTAG exchanger
Resistor	ERX1SJ 1R0	Panasonic	2	Appended part
Resistor	ERX1SJ 1R2	Panasonic	2	Appended part
Resistor	ERX1SJ 1R5	Panasonic	2	Appended part
Resistor	ERX1SJ 1R8	Panasonic	2	Appended part
Resistor	ERX1SJ 2R2	Panasonic	2	Appended part
Resistor	ERX1SJ 2R7	Panasonic	2	Appended part
Resistor	ERX1SJ 3R3	Panasonic	2	Appended part
Resistor	ERX1SJ 3R9	Panasonic	2	Appended part
Resistor	ERX1SJ 4R7	Panasonic	2	Appended part
Resistor	ERX1SJ 5R6	Panasonic	2	Appended part
Resistor	ERX1SJ 6R8	Panasonic	2	Appended part
Resistor	ERX1SJ 8R2	Panasonic	2	Appended part

Components in RED are not mounted.

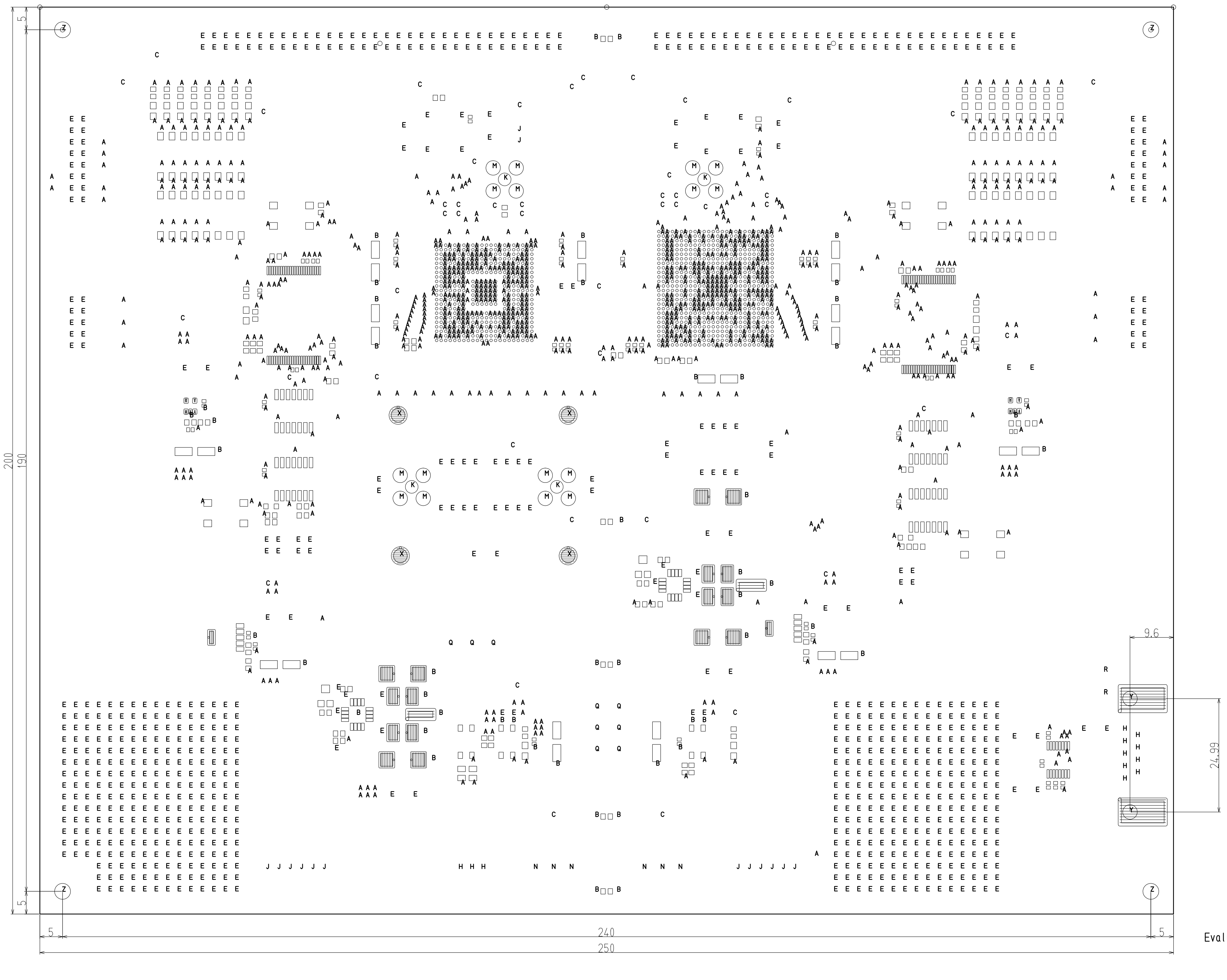
7. Board Information

Specification of the Printed Circuit Board:

Board dimension	---	250 mm x 200 mm x 1.6 mm
Number of layers	---	8 layers
Board material	---	FR-4

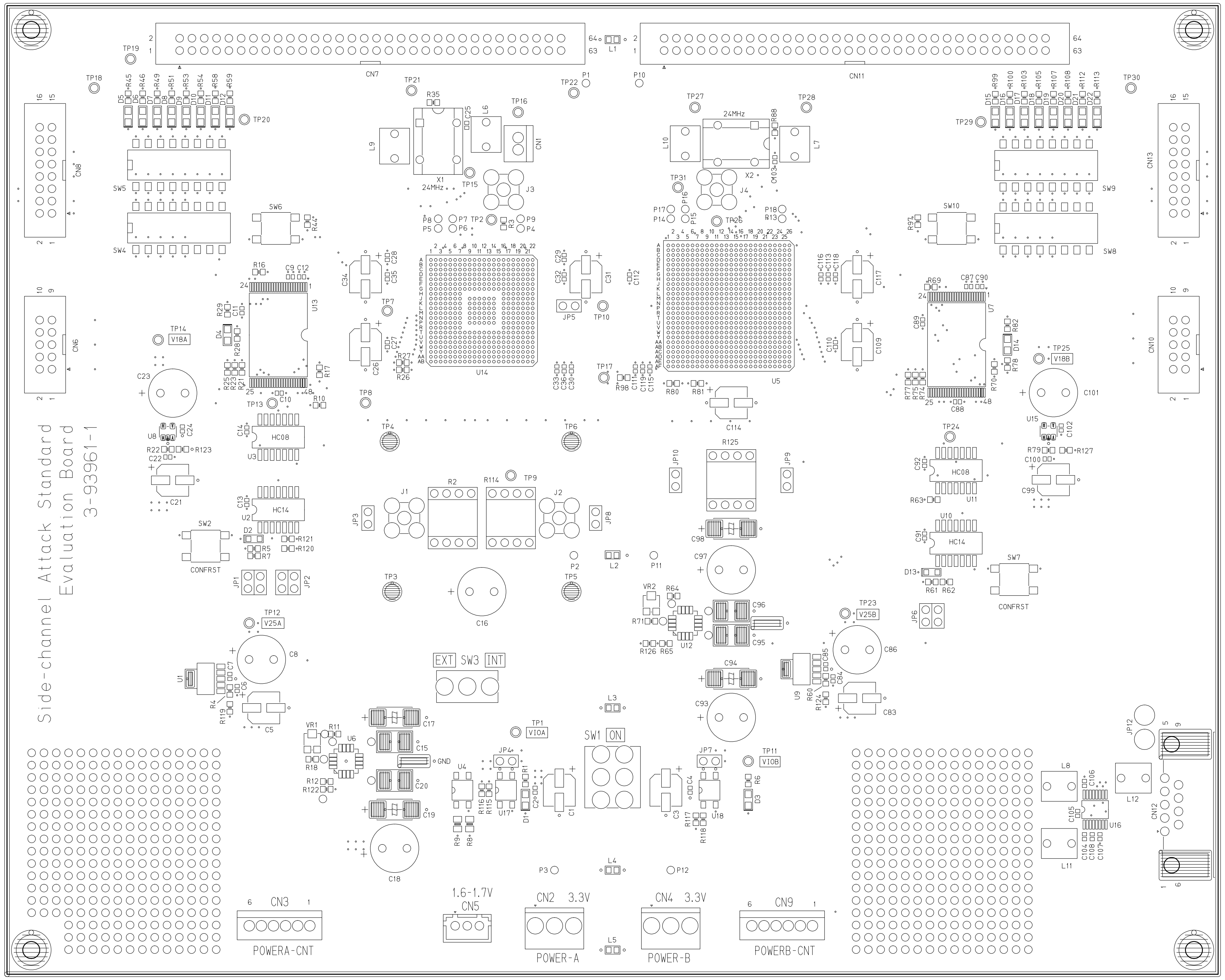
Board Layout Images:

Dimensional drawing	-----	p.26
Part-side drawing	-----	p.27
Solder-side drawing	-----	p.28
Part-side silk screen	-----	p.29
Solder-side silk screen	-----	p.30



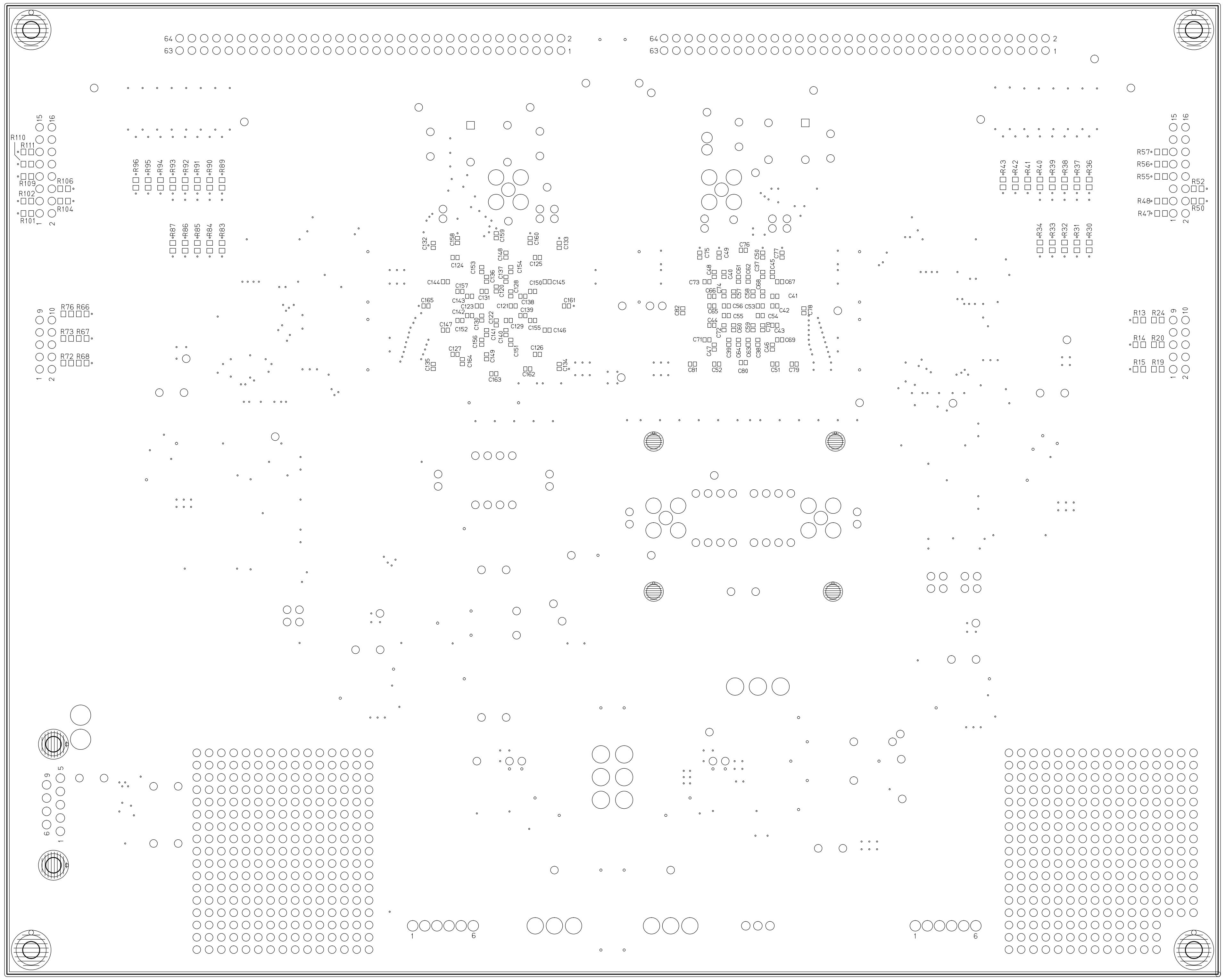
form	diameter	number
X	1.6000	4
Y	3.2000	2
Z	3.5000	4
A	0.3000	1027
B	0.5000	50
C	0.8000	45
E	0.9000	796
H	1.0000	12
J	1.2000	14
K	1.5000	4
M	1.7000	16
N	1.8000	6
Q	1.9000	9
R	2.0000	2

Evaluation Board
2007/02/13



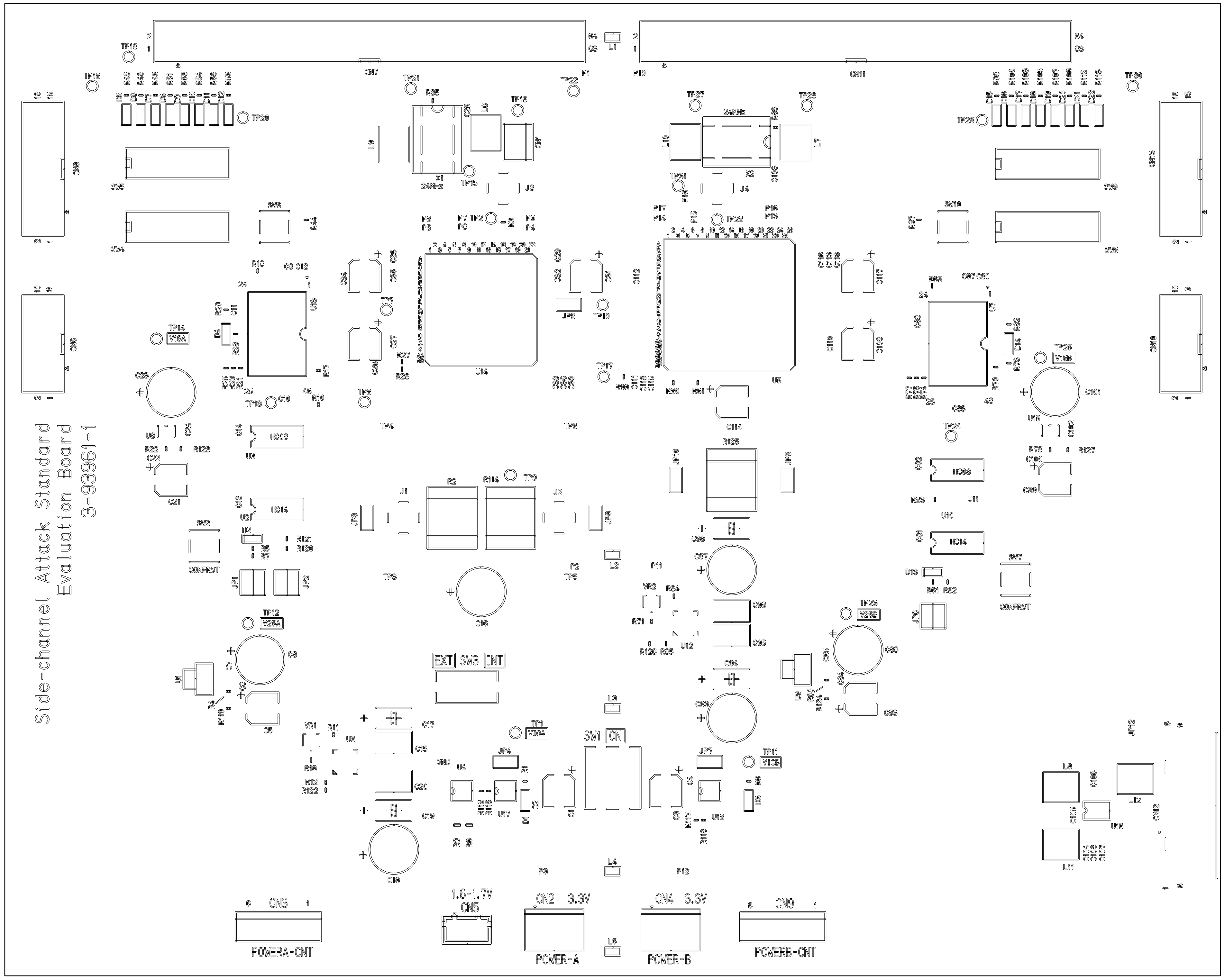
CS

Evaluation Board
2007/02/13



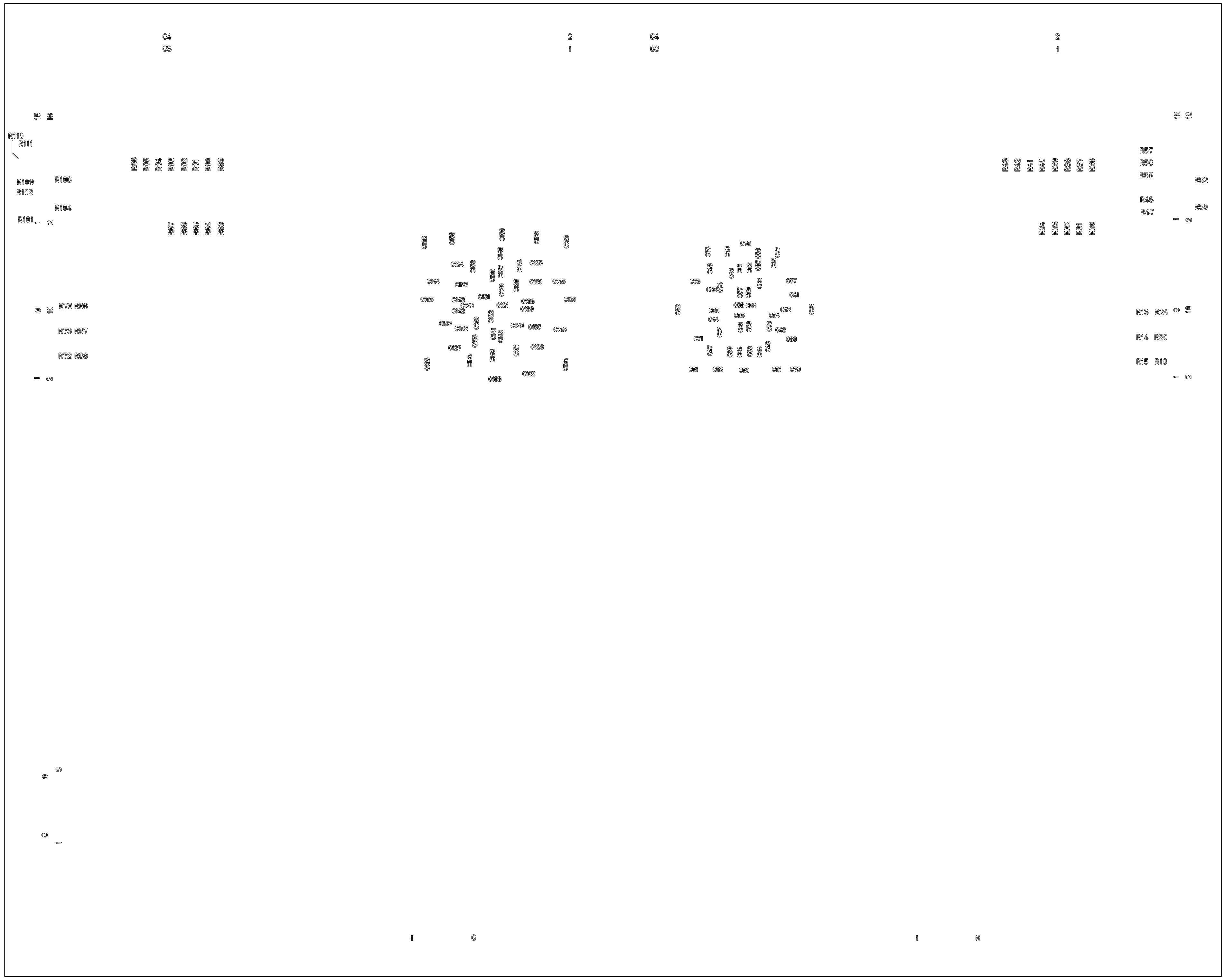
SS

Evaluation Board
2007/02/13



CS

Evaluation Board
2007/02/13



Evaluation Board
2007/02/13

8. How to Write Configuration Data to Flash ROM

<Environments>

- ISE must be installed on the host PC.
- A Xilinx download cable is used.
- A proper driver for the download cable is installed in the PC.

<Cable connection>

1. Connect the Xilinx download cable to the PC.
2. Attach a 10-pin to 14-pin conversion connector to the board.
3. Connect the Xilinx download cable and the board with a 14-pin cable.

<Flash ROM data generation>

A Flash ROM data file (MCS) is created by converting a bit stream file with the Xilinx iMPACT tool.

1. Launch iMPACT.
2. Specify the proper project name and location.
3. Select “Prepare a PROM file” from the iMPACT menu, and then press the Next button.
4. Select “Xilinx PROM” as the target and “MCS” as the PROM file format. Enter the file location in the “Location” field, and optionally specify the name of the file in “PROM File Name” field. Press the Next button to go to the next menu.
5. Choose a proper PROM device (xcf08p for the target FPGA or xcf16p for the control FPGA) from the pull-down menu. Press the Add button to add a device and then press the Next button.
6. Check the radio button “File Generation Summary” and click the “Finish” button.
7. The “Add device” menu will appear. Click the “Yes” button.
8. Specify the bit stream file (*.bit) to be converted into the MCS file.
9. The “Add device” menu will appear. However, since there is no device to create a PROM file, select “No” and then click the “OK” button.
10. In the “iMPACT Processes” menu on the left side of the iMPACT window, double click the “Generate File”. The MCS file will be generated.
11. When the message “PROM File Generation Succeeded” appears, the MCS file has been successfully generated.

<PROM file downloading>

1. Launch iMPACT.
2. Select “Configure devices using Boundary-Scan (JTAG)” and click the Finish button.
3. When the message “Identify Succeeded” appears, specify the bit stream file to be configured.
4. If you want to replace the assigned bit stream, click the right button on your mouse and select “Assign New Configuration file”.
5. Right click and select “Program”. Optionally, check the “verify mode” and/or other program properties. Press the “OK” button Configuration of the device will start.
6. If the message “Program Succeeded” appears, the device is successfully configured.

9. Reference

[1]Xilinx, "Virtex-II Pro and Virtex-II Pro X FPGA User Guide"
[2]Xilinx, "Virtex-II Pro PowerPC Example Design"

*4 The specifications of this product are subject to revision without notice.

Technical inquiries:

National Institute of Advanced Industrial Science and Technology (AIST)
Research Center for Information Security (RCIS)

Akihabara-Daibiru 11F Room 1102
1-18-13 Sotokanda, Chiyoda-ku, Tokyo, 101-0021 Japan
TEL: +81-3-5298-4722
FAX: +81-3-5298-4522