SAKURA-G

Side-channel AttacK User Reference Architecture

Specifications

Version 1.0
August 1, 2013

SAKURA Hardware Security Project

MORITA TECH CO., LTD.

Revision History

The following table shows the revision history.

Date	Version	Revision
2013-08-01	1.0	Initial release.

Table of Contents

1. Overview

The SAKURA-G FPGA board is designed for research and development on hardware security, such as Side-Channel Attacks (SCA), Fault Injection Attacks (FIA), Physical Unclonable Functions (PUF), and dynamic reconfiguration. Two Spartan-6 FPGAs are integrated on the board and serve as the controller and main security circuits, respectively. SAKURA-G is highly compatible with SASEBO-GII. A Spartan-6 LX75 provides a logic circuit 2.5 times larger than the Virtex-5 LX30 on SASEBO-GII. Ultra-low-noise board design and an on-board amplifier make power analysis easier. Users can easily configure and operate SAKURA-G using Verilog-HDL code designed for SASEBO-GII and the free Xilinx ISE WebPACK design software.

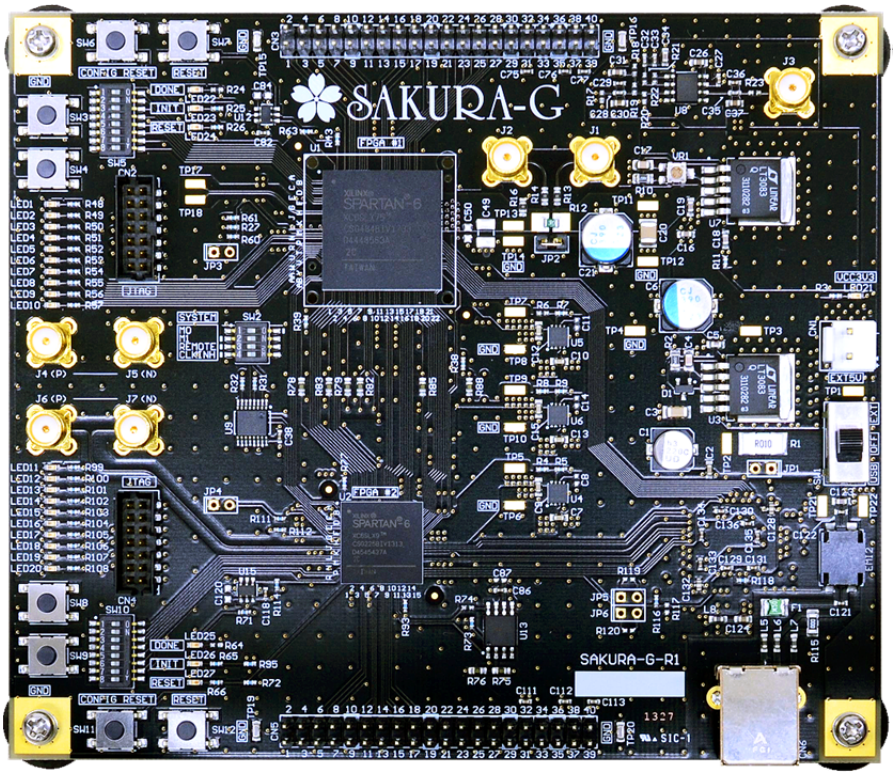


Figure 1 : SAKURA-G Board Overview (Top View)

Table 1 : Key Specifications

FPGA #1 (Main)	FPGA	・Xilinx Spartan-6 (XC6SLX75-2CSG484C)
	Configuration ROM	・32Mbit SPI-ROM (Atmel/Adesto AT45DB321D)
	Configuration Mode	・JTAG ・from SPI-ROM : Master SPI (x1) ・from Controller FPGA : Master Serial / Master SPI (x1, x2, x4) / Master SelectMAP (x8) / Slave SelectMAP (x8) / Slave Serial
	Clock	・48.000MHz Clock Oscillator
	Reset	・210ms(typ.)-delayed reset signal from DONE ・Manual Reset (Push switch)
	User LED	・10 bit
	User switch	・2 bit Push switches ・8 bit DIP switch
	User GPIO	・26 bit Header ・2 ports SMA (2 single ended or 1 differential pair, clock capable)
	USB I/F	・FTDI FT2232H Channel B
	Measurement point	・High side of VCCINT (Core)
	Amplifier	・360MHz Bandwidth, +20dB Gain (+14dB for 50ohm termination)
FPGA #2 (Controller)	FPGA	・Xilinx Spartan-6 (XC6SLX9-2CSG225C)
	Configuration ROM	・32Mbit SPI-ROM Atmel/Adesto AT45DB321D
	Clock	・48.000MHz Clock Oscillator
	Reset	・210ms(typ.)-delayed reset signal from DONE ・Manual Reset (Push switch)
	User LED	・10 bit
	User switch	・2 bit Push switch ・8 bit DIP switch
	User GPIO	・26 bit Header ・2 ports SMA (2 single ended or 1 differential pair, clock capable)
	USB I/F	・FTDI FT2232H Channel A
	FPGA Interconnect	・51 bit
	Rated voltage	・5V ±5%
	Rated current	・500mA via USB (Protected by resettable fuse) ・3A via External Power Supply (Rated by LDO)
	Circuit board	・6 Layers, FR-4, 1.6t
	Dimensions	・140mm × 120mm

2. Operational Instructions

Figure 2 and Figure 3 show the functions of the each part on the SAKURA-G board. Figure 4 shows the functions as block diagram.

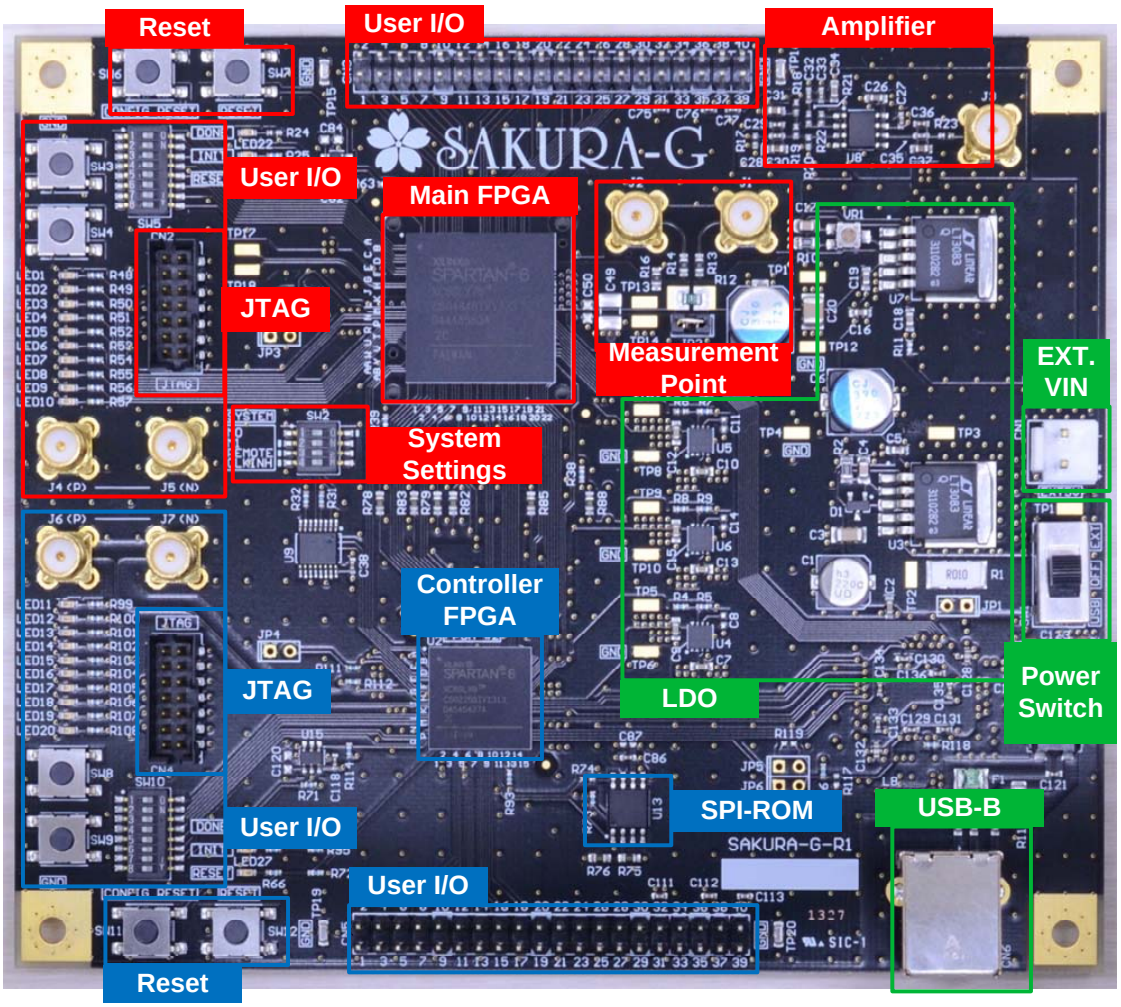


Figure 2 : SAKURA-G Board Functions (Top View)

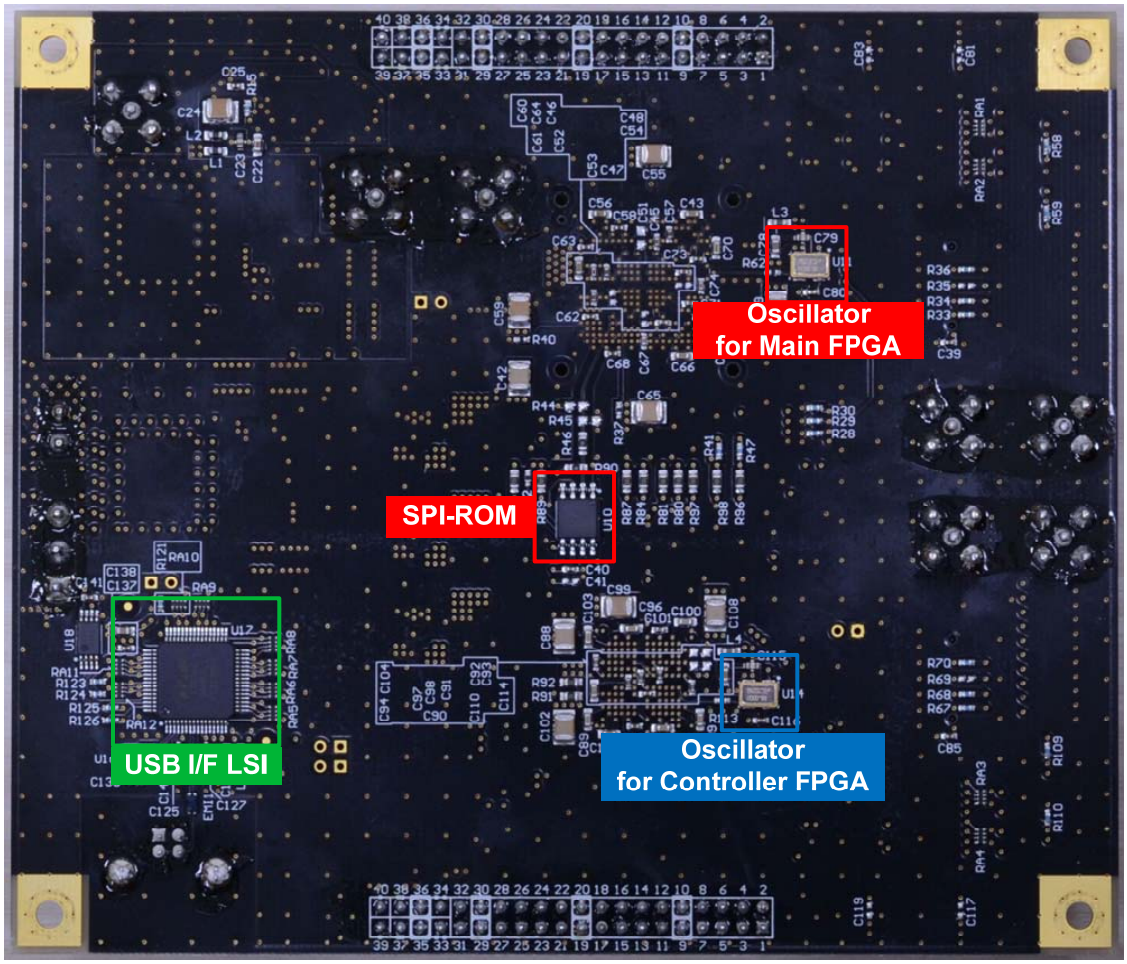


Figure 3 : SAKURA-G Board Functions (Bottom View)

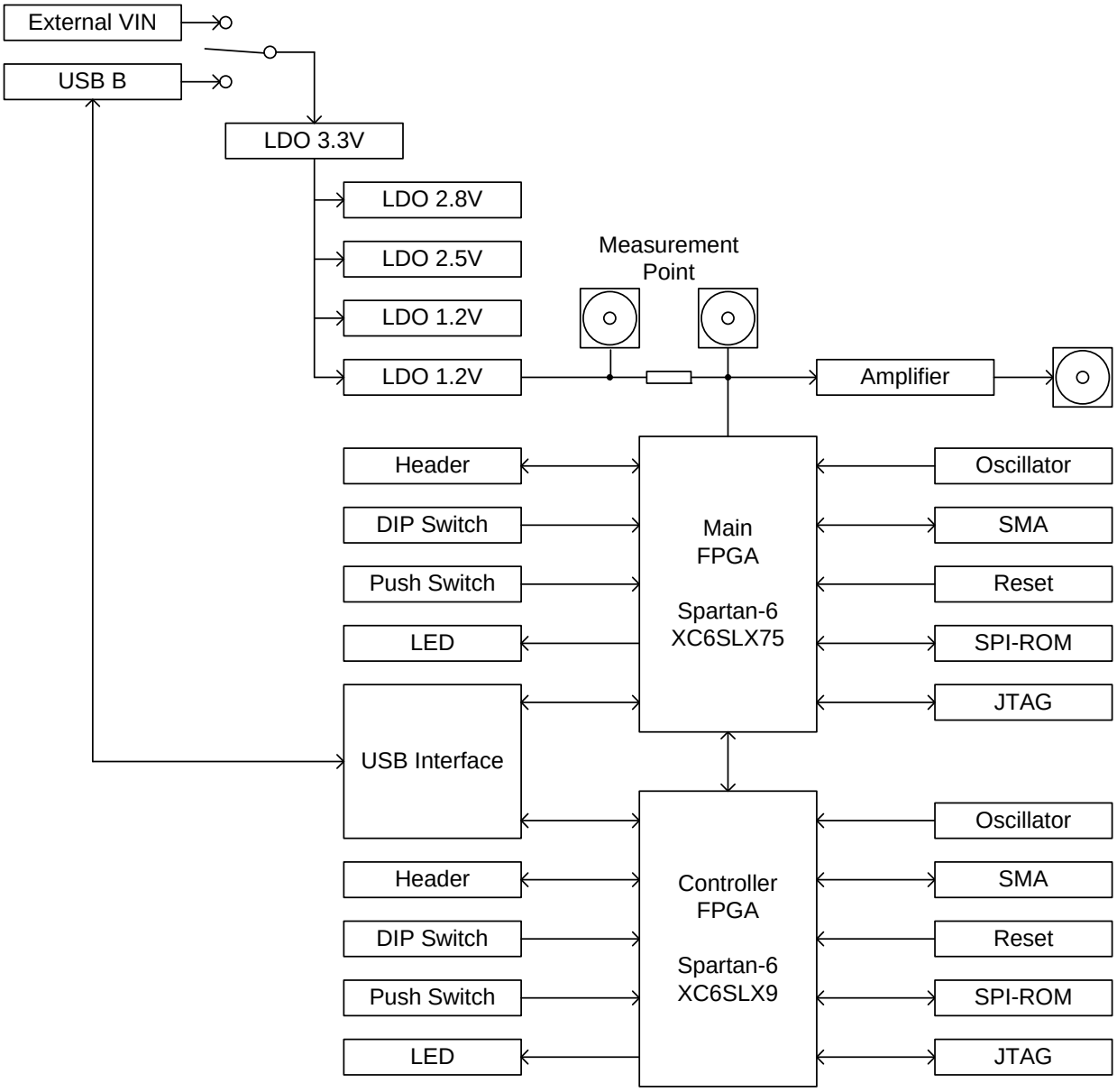


Figure 4 : SAKURA-G Functional Block Diagram

2.1. Power Circuit

The recommended source voltage (EXT 5.0V) range is between 4.75V and 5.25V. The absolute maximum rating of input voltage is 12.6V, limited by amplifier AD8000.

2.1.1. Block Diagram

The power supply can be selected to come from the USB B connector (CN6) or the External 5.0V connector (CN1) by toggling Power Switch (SW1).

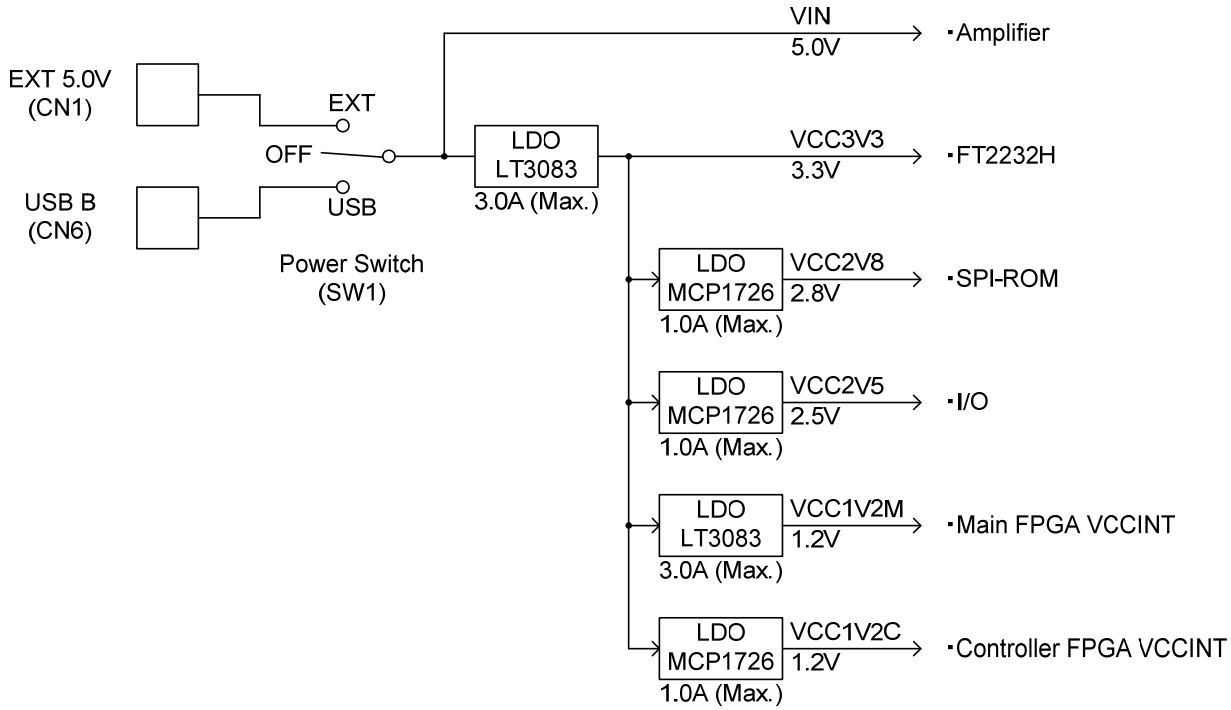


Figure 5 : Power System

2.1.2. Power-On Sequence

As shown in Figure 6, FPGA configuration starts when voltages VCC2V5 and VCC1V2 rise according to the power-on reset sequence. When the configuration is completed, a supervisor IC holds the software reset signal low for 210ms.

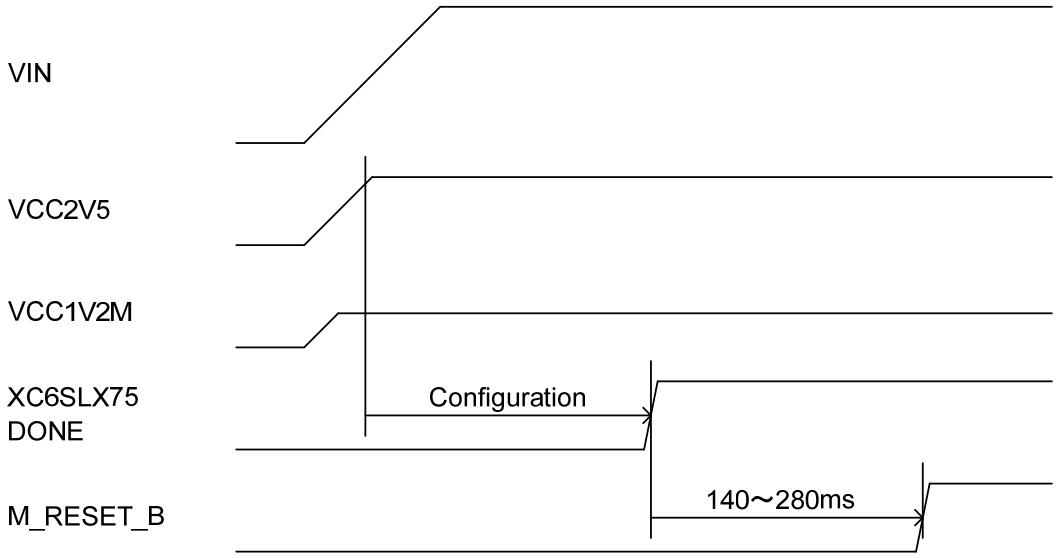


Figure 6 : Power-On Sequence of Main FPGA

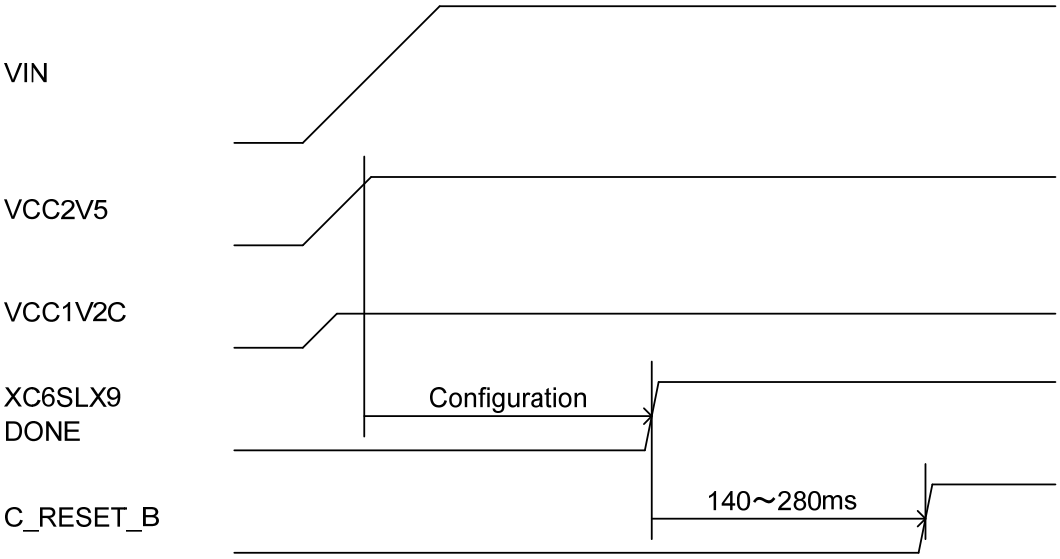


Figure 7 : Power-On Sequence of Controller FPGA

2.1.3. Voltage Calibration

The voltage of VCC1V2M (core voltage for the nain FPGA) can be adjusted from 0.5 – 1.5V by using trimmer VR1. Shorting JP2 with a jumper can prevent voltage drop at VCCINT when large power consumption is required.

2.2. Configuration

The controller FPGA should be configured before the main FPGA by setting DIP switch SW2 to an appropriate position, excepting in cases where the main FPGA is configured using a JTAG chain.

2.2.1. JTAG Chain

Each FPGA has its own JTAG chain. The JTAG connectors, CN2 and CN4, are connected to the main FPGA U1 and the controller FPGA U2, respectively. SPI-ROMs are not connected to these JTAG chain.

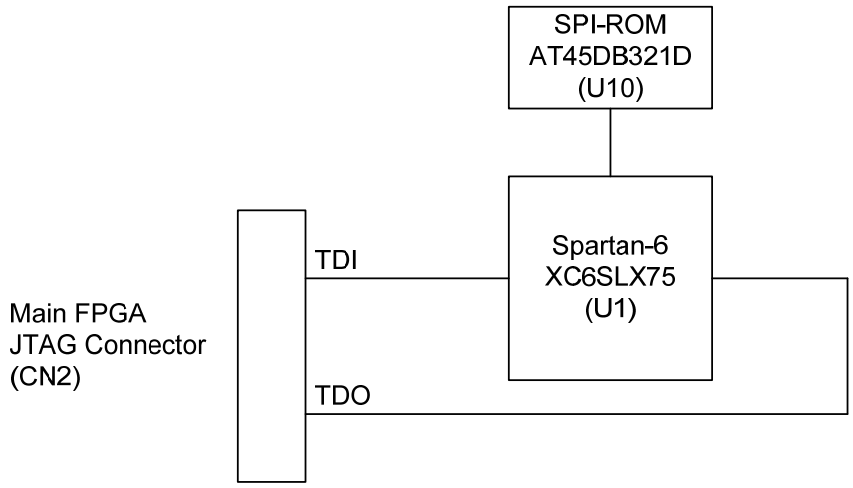


Figure 8 : JTAG Chain for Main FPGA

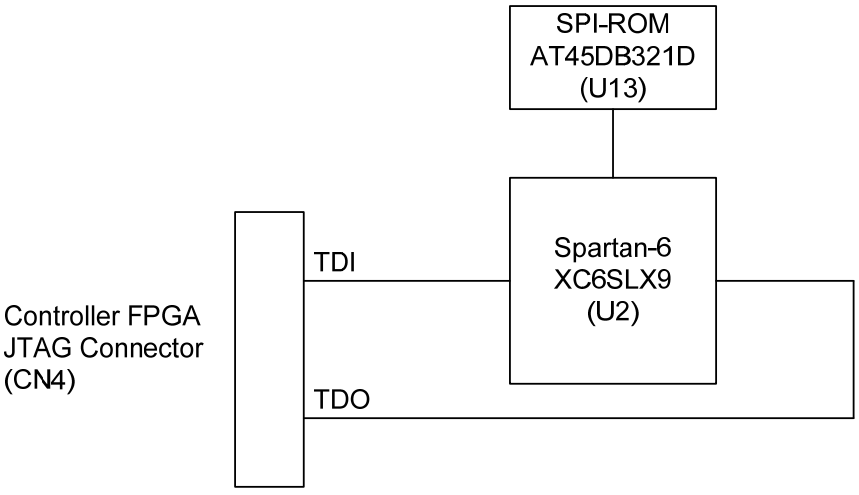


Figure 9 : JTAG Chain for Controller FPGA

2.2.2. Configuration Mode

The configuration mode pins M0 and M1 of the main FPGA can be set using DIP switch SW2 or the controller FPGA. Only DIP switch SW2-1 should be set to high when configuring the main FPGA from the SPI-ROM.

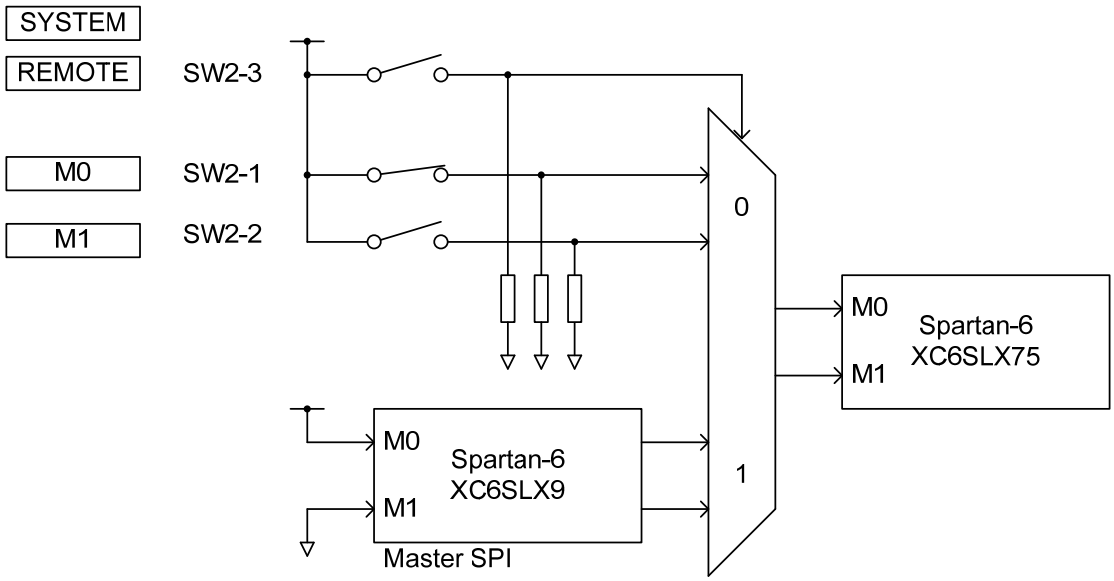


Figure 10 : Configuration Mode Settings

2.2.3. Remote Configuration

The configuration pins of the main FPGA are connected to the controller FPGA. When remote configuration is not used, all configuration signals should be set to pull-up or float to avoid failing the configuration process.

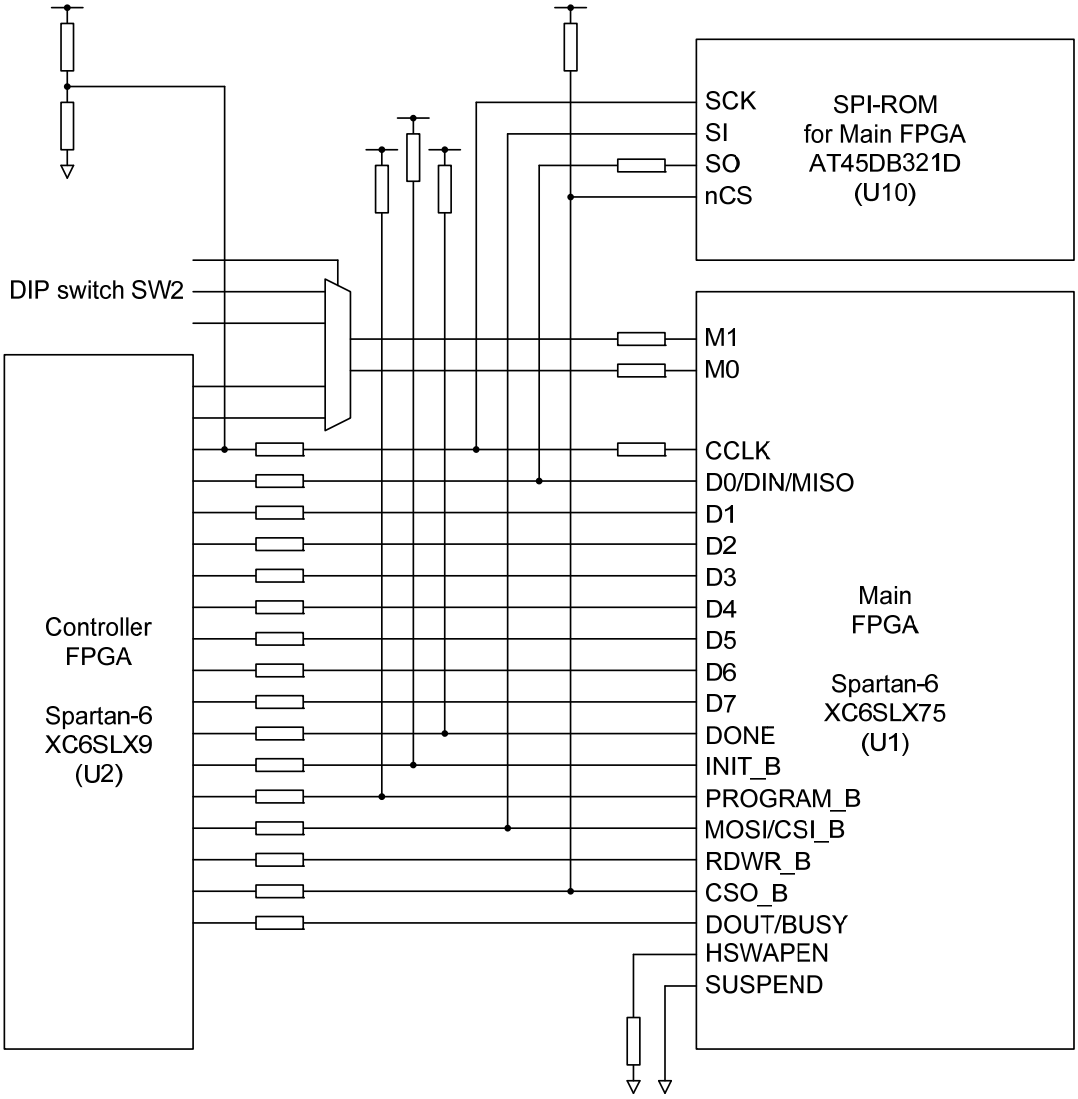
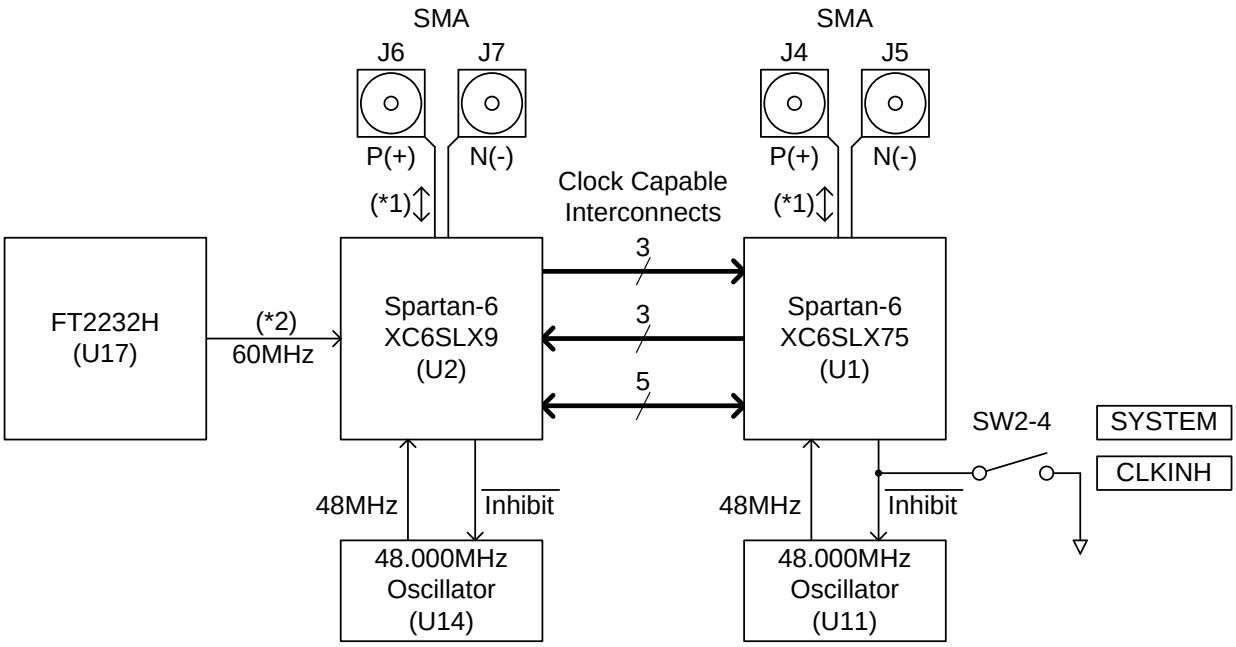


Figure 11 : Configuration Signals of Main FPGA

2.3. Clock System

Each FPGA has each own on-board 48MHz clock oscillator. The oscillators can be disabled when the FPGAs use external clocks through two pairs of SMA connectors. The USB Interface chip FTDI FT2232H supplies 60MHz clock when the chip is operated in a synchronous FIFO mode.



(*1) 1 differential pair or 2 single ended
(*2) This clock signal is only available when using "FT245 Synchronous FIFO Interface Mode".

Figure 12 : Clock System

2.4. Measurement Points

Two measurement points, SMA connectors J1 and J2 are available to monitor power waveforms on the core voltage VCCINT of the main FPGA as shown in Figure 13. The current-sense resistor R12 can be bypassed by inserting a jumper into JP2. SMA connector J3 outputs the amplified waveform.

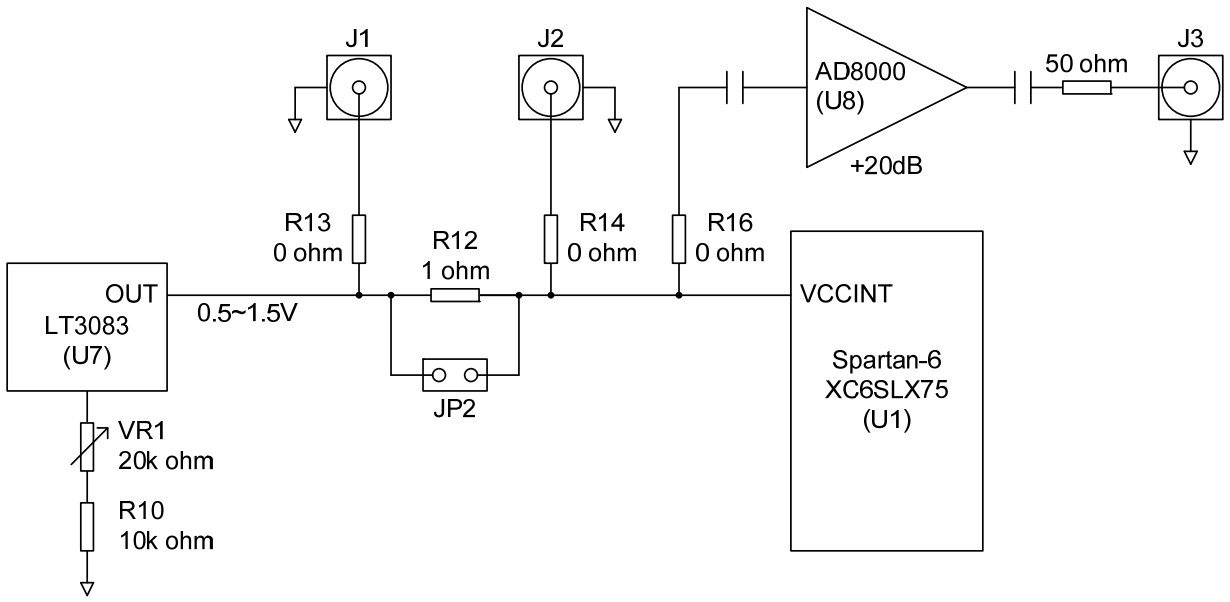


Figure 13 : Measurement Points

2.5. USB Interface

Channel A of the FT2232H is connected to the controller FPGA and channel B is connected to the main FPGA. The reset pin of the FT2232H is simply pulled up.

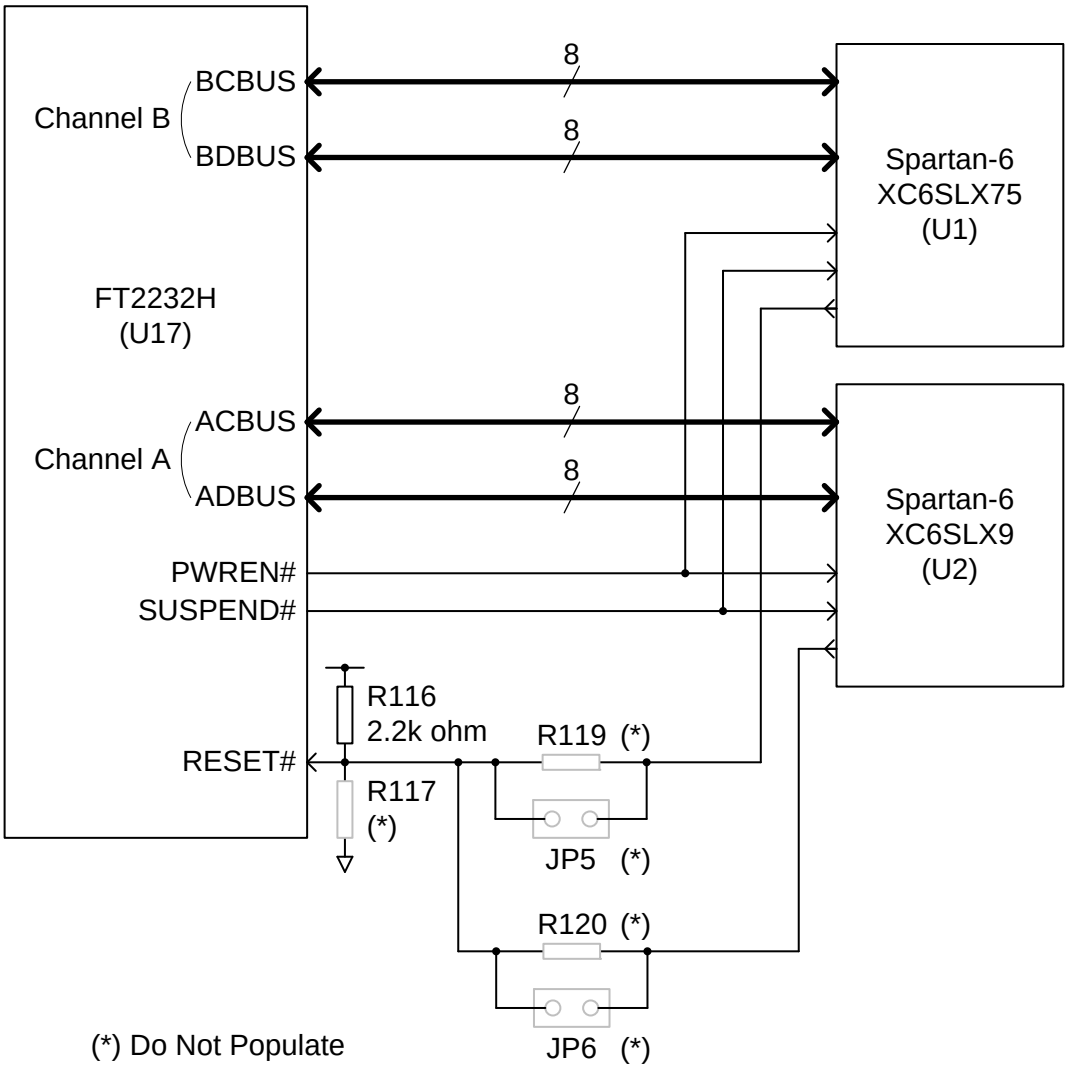


Figure 14 : USB Interface

2.6. I/O

2.6.1. Connectors

Table 2 : SAKURA-G Connectors

Designator	Function
CN1	External Power Supply (5.0V)
CN2	JTAG for Main FPGA
CN3	Header for Main FPGA
CN4	JTAG for Controller FPGA
CN5	Header for Controller FPGA
CN6	USB
J1	High-side current-sense resistor for Main FPGA (Regulator IC side)
J2	High-side current-sense resistor for Main FPGA (FPGA side)
J3	Amplified J2
J4	Differential-clock capable SMA user I/O for Main FPGA (Positive)
J5	Differential-clock capable SMA user I/O for Main FPGA (Negative)
J6	Differential-clock capable SMA user I/O for Controller FPGA (Positive)
J7	Differential-clock capable SMA user I/O for Controller FPGA (Negative)

Table 3 : CN1 – External Power Supply

Pin	Function
1 (▲)	External 5.0V (EXT_VCC5V)
2	GND

Table 4 : CN2 – JTAG for Main FPGA

Pin	Function
1	GND
2	2.5V (VCC2V5)
3	GND
4	TMS
5	GND
6	TCK
7	GND
8	TDO
9	GND

10	TDI
11	GND
12	N.C.
13	GND
14	N.C.

Table 5 : CN3 – Header for Main FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	User GPIO	M_HEADER_0	A4	2.5V
2	User GPIO	M_HEADER_1	A5	2.5V
3	User GPIO	M_HEADER_2	B6	2.5V
4	User GPIO	M_HEADER_3	A6	2.5V
5	User GPIO	M_HEADER_4	A7	2.5V
6	User GPIO	M_HEADER_5	B8	2.5V
7	User GPIO	M_HEADER_6	A8	2.5V
8	User GPIO	M_HEADER_7	A9	2.5V
9	GND	GND		
10	GND	GND		
11	User GPIO	M_HEADER_8	C5	2.5V
12	User GPIO	M_HEADER_9	C6	2.5V
13	User GPIO	M_HEADER_10	C7	2.5V
14	User GPIO	M_HEADER_11	C17	2.5V
15	User GPIO (Clock Capable)	M_HEADER_12	A11	2.5V
16	User GPIO (Clock Capable)	M_HEADER_13	A12	2.5V
17	User GPIO (Clock Capable)	M_HEADER_14	B12	2.5V
18	User GPIO	M_HEADER_15	A13	2.5V
19	GND	GND		
20	GND	GND		
21	User GPIO	M_HEADER_16	A14	2.5V
22	User GPIO	M_HEADER_17	B14	2.5V
23	User GPIO	M_HEADER_18	A15	2.5V
24	User GPIO	M_HEADER_19	A16	2.5V
25	User GPIO	M_HEADER_20	B16	2.5V
26	User GPIO	M_HEADER_21	A17	2.5V
27	User GPIO	M_HEADER_22	A18	2.5V
28	User GPIO	M_HEADER_23	B18	2.5V

29	GND	GND		
30	GND	GND		
31	User GPIO (Clock Capable)	M_HEADER_CLK_P	B10	2.5V
32	User GPIO (Clock Capable)	M_HEADER_CLK_N	A10	2.5V
33	2.5V power supply	VCC2V5		
34	2.5V power supply	VCC2V5		
35	GND	GND		
36	GND	GND		
37	3.3V power supply	VCC3V3		
38	3.3V power supply	VCC3V3		
39	VIN power supply	VIN		
40	VIN power supply	VIN		

Table 6 : CN4 – JTAG for Controller FPGA

Pin	Function
1	GND
2	2.5V (VCC2V5)
3	GND
4	TMS
5	GND
6	TCK
7	GND
8	TDO
9	GND
10	TDI
11	GND
12	N.C.
13	GND
14	N.C.

Table 7 : CN5 – Header for Controller FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	User GPIO	C_HEADER_0	N4	2.5V
2	User GPIO	C_HEADER_1	M5	2.5V
3	User GPIO	C_HEADER_2	N5	2.5V
4	User GPIO	C_HEADER_3	M6	2.5V

5	User GPIO	C_HEADER_4	N6	2.5V
6	User GPIO	C_HEADER_5	R4	2.5V
7	User GPIO	C_HEADER_6	P5	2.5V
8	User GPIO	C_HEADER_7	R5	2.5V
9	GND	GND		
10	GND	GND		
11	User GPIO	C_HEADER_8	R6	2.5V
12	User GPIO (Clock Capable)	C_HEADER_9	P7	2.5V
13	User GPIO (Clock Capable)	C_HEADER_10	R7	2.5V
14	User GPIO (Clock Capable)	C_HEADER_11	R8	2.5V
15	User GPIO (Clock Capable)	C_HEADER_12	N8	2.5V
16	User GPIO	C_HEADER_13	R9	2.5V
17	User GPIO	C_HEADER_14	P9	2.5V
18	User GPIO	C_HEADER_15	R10	2.5V
19	GND	GND		
20	GND	GND		
21	User GPIO	C_HEADER_16	L5	2.5V
22	User GPIO	C_HEADER_17	L6	2.5V
23	User GPIO (Clock Capable)	C_HEADER_18	L8	2.5V
24	User GPIO	C_HEADER_19	M9	2.5V
25	User GPIO	C_HEADER_20	N9	2.5V
26	User GPIO	C_HEADER_21	M10	2.5V
27	User GPIO	C_HEADER_22	N11	2.5V
28	User GPIO	C_HEADER_23	M11	2.5V
29	GND	GND		
30	GND	GND		
31	User GPIO (Clock Capable)	C_HEADER_CLK_N	N7	2.5V
32	User GPIO (Clock Capable)	C_HEADER_CLK_P	M8	2.5V
33	2.5V power supply	VCC2V5		
34	2.5V power supply	VCC2V5		
35	GND	GND		
36	GND	GND		
37	3.3V power supply	VCC3V3		
38	3.3V power supply	VCC3V3		
39	VIN power supply	VIN		
40	VIN power supply	VIN		

Table 8 : CN6 – USB

Pin	Function
1	VBUS
2	D-
3	D+
4	GND

Table 9 : J1 – High-side current-sense resistor for Main FPGA (Regulator IC side)

Pin	Function
Center	Signal
Shield	GND

Table 10 : J2 – High-side current-sense resistor for Main FPGA (FPGA side)

Pin	Function
Center	Signal
Shield	GND

Table 11 : J3 – Amplified J2

Pin	Function
Center	Signal
Shield	GND

Table 12 : J4 – Differential-clock capable SMA user I/O for Main FPGA (Positive)

Pin	Function
Center	Signal
Shield	GND

Table 13 : J5 – Differential-clock capable SMA user I/O for Main FPGA (Negative)

Pin	Function
Center	Signal
Shield	GND

Table 14 : J6 – Differential-clock capable SMA user I/O for Controller FPGA (Positive)

Pin	Function
Center	Signal
Shield	GND

Table 15 : J7 – Differential-clock capable SMA user I/O for Controller FPGA (Negative)

Pin	Function
Center	Signal
Shield	GND

2.6.2. Switches

Table 16 : SAKURA-G Switches

Designator	Switch Type	Function
SW1	Slide (SPDT)	Power
SW2	DIP (4bit)	System settings
SW3	Push	User push switch #0 for Main FPGA
SW4	Push	User push switch #1 for Main FPGA
SW5	DIP (8bit)	User DIP switch for Main FPGA
SW6	Push	Reconfiguration for Main FPGA
SW7	Push	Reset for Main FPGA
SW8	Push	User push switch #0 for Controller FPGA
SW9	Push	User push switch #1 for Controller FPGA
SW10	DIP (8bit)	User DIP switch for Controller FPGA
SW11	Push	Reconfiguration for Main FPGA
SW12	Push	Reset for Main FPGA

Table 17 : SW1 – Power

Side	Function
USB	Power supply from USB (USB_VBUS)
OFF	Power off
EXT	Power supply from CN1 (EXT_VCC5V)

Table 18 : SW2 – System settings

Pin	Function	On	Off
1	Mode M0 for Main FPGA	**M0 = 1 (*)**	M0 = 0
2	Mode M1 for Main FPGA	M1 = 1	**M1 = 0 (*)**
3	Mode controller for Main FPGA	Controller FPGA	**SW2-1, SW2-2 (*)**
4	Disable clock oscillator for Main FPGA	Disable	**Enable (*)**

(*): Default settings

Table 19 : SW3 – User push switch #0 for Main FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	Push to High	M_PUSHSW_0	D3	2.5V

Table 20 : SW4 – User push switch #1 for Main FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	Push to High	M_PUSHSW_1	E3	2.5V

Table 21 : SW5 – User DIP switch for Main FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	ON to High	M_DIPSW_0	B2	2.5V
2	ON to High	M_DIPSW_1	B1	2.5V
3	ON to High	M_DIPSW_2	C1	2.5V
4	ON to High	M_DIPSW_3	D2	2.5V
5	ON to High	M_DIPSW_4	D1	2.5V
6	ON to High	M_DIPSW_5	E1	2.5V
7	ON to High	M_DIPSW_6	F2	2.5V
8	ON to High	M_DIPSW_7	F1	2.5V

Table 22 : SW6 – Reconfiguration for Main FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	Push to reconfigure	M_PROG_B	AA1 (*)	2.5V

(*): not for user I/O

Table 23 : SW7 – Reset for Main FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	Push to reset	U12./MR	D3 (U12./RST)	2.5V

Table 24 : SW8 – User push switch #0 for Controller FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	Push to High	C_PUSHSW_0	L3	2.5V

Table 25 : SW9 – User push switch #1 for Controller FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	Push to High	C_PUSHSW_1	M4	2.5V

Table 26 : SW10 – User DIP switch for Controller FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	ON to High	C_DIPSW_0	K1	2.5V
2	ON to High	C_DIPSW_1	L1	2.5V
3	ON to High	C_DIPSW_2	L2	2.5V
4	ON to High	C_DIPSW_3	M1	2.5V
5	ON to High	C_DIPSW_4	N1	2.5V
6	ON to High	C_DIPSW_5	N2	2.5V
7	ON to High	C_DIPSW_6	P1	2.5V
8	ON to High	C_DIPSW_7	M3	2.5V

Table 27 : SW11 – Reconfiguration for Controller FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	Push to reconfigure	C_PROG_B	R2 (*)	2.5V

(*): not for user I/O

Table 28 : SW12 – Reset for Controller FPGA

Pin	Function	Net	FPGA Pin	I/O Voltage
1	Push to reset	U15./MR	P2 (U15./RST)	2.5V

2.6.3. Jumpers

Table 29 : SAKURA-G Jumpers

Designator	Function
JP1 (*)	Current monitor of whole board
JP2	Short when bypassing the current-sense resistor (R12)
JP3 (*)	Short when disable oscillator U11 for Main FPGA
JP4 (*)	Short when disable oscillator U14 for Controller FPGA
JP5 (*)	Short when control FTDI_RESET_B from Main FPGA
JP6 (*)	Short when control FTDI_RESET_B from Controller FPGA

(*) : Optional (Jumper post is not populated)

3. FPGA I/O Assignments

3.1. Main FPGA

Table 30 : Main FPGA (U1) I/O Assignments

Pin	Function	Net	Bank	Voltage
N20	IO_L47P_FWE_B_M1DQ0_1	FTDI_BCBUS0_RXF_B	1	2.5V
P20	IO_L64N_1	FTDI_BCBUS1_TXE_B	1	2.5V
R20	IO_L49P_M1DQ10_1	FTDI_BCBUS2_RD_B	1	2.5V
U20	IO_L51P_M1DQ12_1	FTDI_BCBUS3_WR_B	1	2.5V
V18	IO_L73N_1	FTDI_BCBUS4_SIWUB	1	2.5V
V20	IO_L71N_1	FTDI_BCBUS5	1	2.5V
V19	IO_L71P_1	FTDI_BCBUS6	1	2.5V
W20	IO_L53P_1	FTDI_BCBUS7_PWRSAV_B	1	2.5V
V21	IO_L52P_M1DQ14_1	FTDI_BDBUS0	1	2.5V
V22	IO_L52N_M1DQ15_1	FTDI_BDBUS1	1	2.5V
U22	IO_L51N_M1DQ13_1	FTDI_BDBUS2	1	2.5V
T22	IO_L50N_M1UDQSN_1	FTDI_BDBUS3	1	2.5V
R22	IO_L49N_M1DQ11_1	FTDI_BDBUS4	1	2.5V
P21	IO_L48P_HDC_M1DQ8_1	FTDI_BDBUS5	1	2.5V
P22	IO_L48N_M1DQ9_1	FTDI_BDBUS6	1	2.5V
N22	IO_L47N_LDC_M1DQ1_1	FTDI_BDBUS7	1	2.5V
Y20	IO_L67N_1	FTDI_PWREN_B	1	2.5V
W22	IO_L53N_VREF_1	FTDI_SUSPEND_B	1	2.5V
W1	IO_L9N_3	MC_IC_D0	3	2.5V
Y1	IO_L2N_3	MC_IC_D1	3	2.5V
Y2	IO_L2P_3	MC_IC_D2	3	2.5V
AA2	IO_L1P_3	MC_IC_D3	3	2.5V
AB2	IO_L1N_VREF_3	MC_IC_D4	3	2.5V
AB3	IO_L8N_3	MC_IC_D5	3	2.5V
AA4	IO_L12P_3	MC_IC_D6	3	2.5V
AB4	IO_L12N_3	MC_IC_D7	3	2.5V
AA6	IO_L64P_D8_2	MC_IC_D8	2	2.5V
AB6	IO_L64N_D9_2	MC_IC_D9	2	2.5V
AB11	IO_L31N_GCLK30_D15_2	MC_IC_D10	2	2.5V
AB12	IO_L30N_GCLK0_USERCCLK_2	MC_IC_D11	2	2.5V
AA12	IO_L30P_GCLK1_D13_2	MC_IC_D12	2	2.5V

AB13	IO_L41N_VREF_2	MC_IC_D13	2	2.5V
AB14	IO_L15N_2	MC_IC_D14	2	2.5V
AA14	IO_L15P_2	MC_IC_D15	2	2.5V
AB15	IO_L5N_2	MC_IC_D16	2	2.5V
AB16	IO_L4N_VREF_2	MC_IC_D17	2	2.5V
AA16	IO_L4P_2	MC_IC_D18	2	2.5V
AB18	IO_L2N_CMPMOSI_2	MC_IC_D19	2	2.5V
AA18	IO_L2P_CMPCLK_2	MC_IC_D20	2	2.5V
AB19	IO_L65P_1	MC_IC_D21	1	2.5V
AB20	IO_L65N_1	MC_IC_D22	1	2.5V
AA20	IO_L61P_1	MC_IC_D23	1	2.5V
AB21	IO_L61N_1	MC_IC_D24	1	2.5V
AA21	IO_L63P_1	MC_IC_D25	1	2.5V
AA22	IO_L63N_1	MC_IC_D26	1	2.5V
Y21	IO_L59P_1	MC_IC_D27	1	2.5V
Y22	IO_L59N_1	MC_IC_D28	1	2.5V
V3	IO_L18N_3	MC_IC_D29	3	2.5V
W3	IO_L9P_3	MC_IC_D30	3	2.5V
Y3	IO_L8P_3	MC_IC_D31	3	2.5V
W4	IO_L7P_3	MC_IC_D32	3	2.5V
Y4	IO_L7N_3	MC_IC_D33	3	2.5V
Y7	IO_L63P_2	MC_IC_D34	2	2.5V
Y8	IO_L47N_2	MC_IC_D35	2	2.5V
W9	IO_L47P_2	MC_IC_D36	2	2.5V
AA10	IO_L32P_GCLK29_2	MC_IC_D37	2	2.5V
AB7	IO_L63N_2	MC_IC_D38	2	2.5V
AB10	IO_L32N_GCLK28_2	MC_IC_D39	2	2.5V
Y10	IO_L29N_GCLK2_2	MC_IC_D40	2	2.5V
Y11	IO_L31P_GCLK31_D14_2	MC_IC_D41	2	2.5V
W11	IO_L29P_GCLK3_2	MC_IC_D42	2	2.5V
W12	IO_L42P_2	MC_IC_D43	2	2.5V
Y12	IO_L42N_2	MC_IC_D44	2	2.5V
Y13	IO_L41P_2	MC_IC_D45	2	2.5V
Y14	IO_L16N_VREF_2	MC_IC_D46	2	2.5V
W14	IO_L16P_2	MC_IC_D47	2	2.5V
Y15	IO_L5P_2	MC_IC_D48	2	2.5V

W15	IO_L14P_D11_2	MC_IC_D49	2	2.5V
Y16	IO_L14N_D12_2	MC_IC_D50	2	2.5V
W17	IO_L1P_CCLK_2	M_CCLK_R0	2	2.5V
P3	IO_L43N_GCLK22_IRDY2_M3CASN_3	M_CLK_EXT0_N	3	2.5V
N4	IO_L43P_GCLK23_M3RASN_3	M_CLK_EXT0_P	3	2.5V
M1	IO_L38N_M3DQ3_3	M_CLK_INH_B	3	2.5V
J1	IO_L41N_GCLK26_M3DQ5_3	M_CLK_OSC	3	2.5V
AB5	IO_L65N_CSO_B_2	M_CSO_B	2	2.5V
Y17	IO_L3P_D0_DIN_MISO_MISO1_2	M_D0_DIN_MISO	2	2.5V
V13	IO_L12P_D1_MISO2_2	M_D1	2	2.5V
W13	IO_L12N_D2_MISO3_2	M_D2	2	2.5V
AA8	IO_L49P_D3_2	M_D3	2	2.5V
AB8	IO_L49N_D4_2	M_D4	2	2.5V
W6	IO_L62P_D5_2	M_D5	2	2.5V
Y6	IO_L62N_D6_2	M_D6	2	2.5V
Y9	IO_L48P_D7_2	M_D7	2	2.5V
B2	IO_L54P_M3RESET_3	M_DIPSW_0	3	2.5V
B1	IO_L54N_M3A11_3	M_DIPSW_1	3	2.5V
C1	IO_L52N_M3A9_3	M_DIPSW_2	3	2.5V
D2	IO_L50P_M3WE_3	M_DIPSW_3	3	2.5V
D1	IO_L50N_M3BA2_3	M_DIPSW_4	3	2.5V
E1	IO_L48N_M3BA1_3	M_DIPSW_5	3	2.5V
F2	IO_L46P_M3CLK_3	M_DIPSW_6	3	2.5V
F1	IO_L46N_M3CLKN_3	M_DIPSW_7	3	2.5V
T20	IO_L74N_DOUT_BUSY_1	M_DOUT_BUSY	1	2.5V
Y19	IO_L67P_1	M_FTDI_RESET_B	1	2.5V
A4	IO_L1N_VREF_0	M_HEADER_0	0	2.5V
A5	IO_L2N_0	M_HEADER_1	0	2.5V
B6	IO_L4P_0	M_HEADER_2	0	2.5V
A6	IO_L4N_0	M_HEADER_3	0	2.5V
A7	IO_L5N_0	M_HEADER_4	0	2.5V
B8	IO_L6P_0	M_HEADER_5	0	2.5V
A8	IO_L6N_0	M_HEADER_6	0	2.5V
A9	IO_L8N_VREF_0	M_HEADER_7	0	2.5V
C5	IO_L2P_0	M_HEADER_8	0	2.5V
C6	IO_L3N_0	M_HEADER_9	0	2.5V

C7	IO_L5P_0	M_HEADER_10	0	2.5V
C17	IO_L64P_SCP5_0	M_HEADER_11	0	2.5V
A11	IO_L35N_GCLK16_0	M_HEADER_12	0	2.5V
A12	IO_L36N_GCLK14_0	M_HEADER_13	0	2.5V
B12	IO_L36P_GCLK15_0	M_HEADER_14	0	2.5V
A13	IO_L48N_0	M_HEADER_15	0	2.5V
A14	IO_L50N_0	M_HEADER_16	0	2.5V
B14	IO_L50P_0	M_HEADER_17	0	2.5V
A15	IO_L62N_VREF_0	M_HEADER_18	0	2.5V
A16	IO_L63N_SCP6_0	M_HEADER_19	0	2.5V
B16	IO_L63P_SCP7_0	M_HEADER_20	0	2.5V
A17	IO_L64N_SCP4_0	M_HEADER_21	0	2.5V
A18	IO_L66N_SCP0_0	M_HEADER_22	0	2.5V
B18	IO_L66P_SCP1_0	M_HEADER_23	0	2.5V
A10	IO_L34N_GCLK18_0	M_HEADER_CLK_N	0	2.5V
B10	IO_L34P_GCLK19_0	M_HEADER_CLK_P	0	2.5V
B3	IO_L1P_HSWAPEN_0	M_HSWAPEN	0	2.5V
Y5	IO_L65P_INIT_B_2	M_INIT_B	2	2.5V
M2	IO_L38P_M3DQ2_3	M_LED_0	3	2.5V
N1	IO_L37N_M3DQ1_3	M_LED_1	3	2.5V
P1	IO_L36N_M3DQ9_3	M_LED_2	3	2.5V
P2	IO_L36P_M3DQ8_3	M_LED_3	3	2.5V
R1	IO_L35N_M3DQ11_3	M_LED_4	3	2.5V
T1	IO_L34N_M3UDQSN_3	M_LED_5	3	2.5V
T2	IO_L34P_M3UDQS_3	M_LED_6	3	2.5V
U1	IO_L33N_M3DQ13_3	M_LED_7	3	2.5V
V1	IO_L32N_M3DQ15_3	M_LED_8	3	2.5V
V2	IO_L32P_M3DQ14_3	M_LED_9	3	2.5V
Y18	IO_L1N_M0_CMPMISO_2	M_M0	2	2.5V
U15	IO_L13P_M1_2	M_M1	2	2.5V
AB17	IO_L3N_MOSI_CSI_B_MISO0_2	M_MOSI_CSI_B	2	2.5V
D3	IO_L81N_3	M_PUSHSW_0	3	2.5V
E3	IO_L48P_M3BA0_3	M_PUSHSW_1	3	2.5V
AB9	IO_L48N_RDWR_B_VREF_2	M_RDWR_B	2	2.5V
A2	IO_L83N_VREF_3	M_RESET_B	3	2.5V
H1	IO_L42N_GCLK24_M3LDM_3	M_RSVIO_0_N	3	2.5V

H2	IO_L42P_GCLK25_TRDY2_M3UDM_3	M_RSVIO_0_P	3	2.5V

3.1.1. Clock and Reset

Table 31 : Main FPGA (U1) Clock and Reset

Net	Pin (U1)	Destination	Voltage
M_CLK_OSC	J1	U11.OUT	2.5V
M_CLK_INH_B	M1	U11./INH	2.5V
M_CLK_EXT0_P	N4	J4	2.5V
M_CLK_EXT0_N	P3	J5	2.5V
M_RESET_B	A2	U12./RST	2.5V

3.1.2. User LED

Table 32 : Main FPGA (U1) User LED

Net	Pin (U1)	Destination	Voltage
M_LED_0	M2	LED1	2.5V
M_LED_1	N1	LED2	2.5V
M_LED_2	P1	LED3	2.5V
M_LED_3	P2	LED4	2.5V
M_LED_4	R1	LED5	2.5V
M_LED_5	T1	LED6	2.5V
M_LED_6	T2	LED7	2.5V
M_LED_7	U1	LED8	2.5V
M_LED_8	V1	LED9	2.5V
M_LED_9	V2	LED10	2.5V

3.1.3. User Push switch

Table 33 : Main FPGA (U1) User Push switch

Net	Pin (U1)	Destination	Voltage
M_PUSHSW_0	D3	SW3	2.5V
M_PUSHSW_1	E3	SW4	2.5V

3.1.4. User DIP switch

Table 34 : Main FPGA (U1) User DIP switch

Net	Pin (U1)	Destination	Voltage
M_DIPSW_0	B2	SW5.1	2.5V
M_DIPSW_1	B1	SW5.2	2.5V

M_DIPSW_2	C1	SW5.3	2.5V
M_DIPSW_3	D2	SW5.4	2.5V
M_DIPSW_4	D1	SW5.5	2.5V
M_DIPSW_5	E1	SW5.6	2.5V
M_DIPSW_6	F2	SW5.7	2.5V
M_DIPSW_7	F1	SW5.8	2.5V

3.1.5. User Header

Table 35 : Main FPGA (U1) User Header

Net	Pin (U1)	Destination	Voltage
M_HEADER_0	A4	CN3.1	2.5V
M_HEADER_1	A5	CN3.2	2.5V
M_HEADER_2	B6	CN3.3	2.5V
M_HEADER_3	A6	CN3.4	2.5V
M_HEADER_4	A7	CN3.5	2.5V
M_HEADER_5	B8	CN3.6	2.5V
M_HEADER_6	A8	CN3.7	2.5V
M_HEADER_7	A9	CN3.8	2.5V
M_HEADER_8	C5	CN3.11	2.5V
M_HEADER_9	C6	CN3.12	2.5V
M_HEADER_10	C7	CN3.13	2.5V
M_HEADER_11	C17	CN3.14	2.5V
M_HEADER_12	A11	CN3.15	2.5V
M_HEADER_13	A12	CN3.16	2.5V
M_HEADER_14	B12	CN3.17	2.5V
M_HEADER_15	A13	CN3.18	2.5V
M_HEADER_16	A14	CN3.21	2.5V
M_HEADER_17	B14	CN3.22	2.5V
M_HEADER_18	A15	CN3.23	2.5V
M_HEADER_19	A16	CN3.24	2.5V
M_HEADER_20	B16	CN3.25	2.5V
M_HEADER_21	A17	CN3.26	2.5V
M_HEADER_22	A18	CN3.27	2.5V
M_HEADER_23	B18	CN3.28	2.5V
M_HEADER_CLK_P	B10	CN3.31	2.5V
M_HEADER_CLK_N	A10	CN3.32	2.5V

3.1.6. USB Interface

Table 36 : Main FPGA (U1) USB Interface

Net	Pin (U1)	Destination	Voltage
FTDI_BCBUS0_RXF_B	N20	U17.BCBUS0	2.5V
FTDI_BCBUS1_TXE_B	P20	U17.BCBUS1	2.5V
FTDI_BCBUS2_RD_B	R20	U17.BCBUS2	2.5V
FTDI_BCBUS3_WR_B	U20	U17.BCBUS3	2.5V
FTDI_BCBUS4_SIWUB	V18	U17.BCBUS4	2.5V
FTDI_BCBUS5	V20	U17.BCBUS5	2.5V
FTDI_BCBUS6	V19	U17.BCBUS6	2.5V
FTDI_BCBUS7_PWRSAV_B	W20	U17.BCBUS7	2.5V
FTDI_BDBUS0	V21	U17.BDBUS0	2.5V
FTDI_BDBUS1	V22	U17.BDBUS1	2.5V
FTDI_BDBUS2	U22	U17.BDBUS2	2.5V
FTDI_BDBUS3	T22	U17.BDBUS3	2.5V
FTDI_BDBUS4	R22	U17.BDBUS4	2.5V
FTDI_BDBUS5	P21	U17.BDBUS5	2.5V
FTDI_BDBUS6	P22	U17.BDBUS6	2.5V
FTDI_BDBUS7	N22	U17.BDBUS7	2.5V
FTDI_PWREN_B	Y20	U17.PWREN#	2.5V
FTDI_SUSPEND_B	W22	U17.SUSPEND#	2.5V
M_FTDI_RESET_B	Y19	R119, JP5	2.5V

3.1.7. FPGA Interconnect

Table 37 : FPGA Interconnect between Main FPGA (U1) and Controller FPGA (U2)

Net	Pin (U1)	Pin (U2)	Voltage
MC_IC_D0	W1	D1	2.5V
MC_IC_D1	Y1	C1	2.5V
MC_IC_D2	Y2	C2	2.5V
MC_IC_D3	AA2	B3	2.5V
MC_IC_D4	AB2	A3	2.5V
MC_IC_D5	AB3	A4	2.5V
MC_IC_D6	AA4	B5	2.5V
MC_IC_D7	AB4	A5	2.5V
MC_IC_D8	AA6	B7	2.5V

MC_IC_D9	AB6	A7	2.5V
MC_IC_D10	AB11	A8	2.5V
MC_IC_D11	AB12	A9	2.5V
MC_IC_D12	AA12	B9	2.5V
MC_IC_D13	AB13	A10	2.5V
MC_IC_D14	AB14	A11	2.5V
MC_IC_D15	AA14	B11	2.5V
MC_IC_D16	AB15	A12	2.5V
MC_IC_D17	AB16	A13	2.5V
MC_IC_D18	AA16	B13	2.5V
MC_IC_D19	AB18	B15	2.5V
MC_IC_D20	AA18	C14	2.5V
MC_IC_D21	AB19	C15	2.5V
MC_IC_D22	AB20	D15	2.5V
MC_IC_D23	AA20	E14	2.5V
MC_IC_D24	AB21	E15	2.5V
MC_IC_D25	AA21	F15	2.5V
MC_IC_D26	AA22	G14	2.5V
MC_IC_D27	Y21	G15	2.5V
MC_IC_D28	Y22	H15	2.5V
MC_IC_D29	V3	G3	2.5V
MC_IC_D30	W3	F4	2.5V
MC_IC_D31	Y3	F3	2.5V
MC_IC_D32	W4	F5	2.5V
MC_IC_D33	Y4	E3	2.5V
MC_IC_D34	Y7	D5	2.5V
MC_IC_D35	Y8	C5	2.5V
MC_IC_D36	W9	E6	2.5V
MC_IC_D37	AA10	D7	2.5V
MC_IC_D38	AB7	C8	2.5V
MC_IC_D39	AB10	D8	2.5V
MC_IC_D40	Y10	E7	2.5V
MC_IC_D41	Y11	E8	2.5V
MC_IC_D42	W11	E9	2.5V
MC_IC_D43	W12	D10	2.5V
MC_IC_D44	Y12	C10	2.5V

MC_IC_D45	Y13	C11	2.5V
MC_IC_D46	Y14	D11	2.5V
MC_IC_D47	W14	C12	2.5V
MC_IC_D48	Y15	G12	2.5V
MC_IC_D49	W15	D13	2.5V
MC_IC_D50	Y16	F12	2.5V

3.1.8. Main FPGA Configuration

Table 38 : Main FPGA (U1) Configuration

Net (U1)	Pin (U1)	Net (U2)	Pin (U2)	Other	Voltage
M_CCLK_R0	W17	M_CCLK_R	H13	U10.SCK	2.5V
M_CSO_B	AB5	M_CSO_B_R	A6	U10./CS	2.5V
M_D0_DIN_MISO	Y17	M_D0_DIN_MISO_R	G13	U10.SO	2.5V
M_D1	V13	M_D1_R	C9		2.5V
M_D2	W13	M_D2_R	F11		2.5V
M_D3	AA8	M_D3_R	C4		2.5V
M_D4	AB8	M_D4_R	C6		2.5V
M_D5	W6	M_D5_R	D3		2.5V
M_D6	Y6	M_D6_R	D4		2.5V
M_D7	Y9	M_D7_R	D6		2.5V
M_DONE	U16	M_DONE_R	F13	U12.RSTIN	2.5V
M_DOUT_BUSY	T20	M_DOUT_BUSY_R	G11		2.5V
M_HSWAPEN	B3			R43 (Pull-down)	2.5V
M_INIT_B	Y5	M_INIT_B_R	E4		2.5V
M_M0	Y18			U9.1Y	2.5V
		M_M0_REMOTE	E2	U9.1B	2.5V
M_M1	U15			U9.2Y	2.5V
		M_M1_REMOTE	E1	U9.2B	2.5V
M_MOSI_CSI_B	AB17	M_MOSI_CSI_B_R	B14	U10.SI	2.5V
M_PROG_B	AA1	M_PROG_B_R	A2	SW6	2.5V
M_RDWR_B	AB9	M_RDWR_B_R	C7		2.5V

3.1.9. Reserved I/O

Table 39 : Main FPGA (U1) Reserved I/O

Net	Pin (U1)	Destination	Voltage
M_RSVIO_0_P	H2	TP17	2.5V
M_RSVIO_0_N	H1	TP18	2.5V

3.2. Controller FPGA

Table 40 : Controller FPGA (U2) I/O Assignments

Pin	Function	Net	Bank	Voltage
N12	IO_L1P_CCLK_2	C_CCLK	2	2.5V
J1	IO_L41N_GCLK26_M3DQ5_3	C_CLK_EXT0_N	3	2.5V
J2	IO_L41P_GCLK27_M3DQ4_3	C_CLK_EXT0_P	3	2.5V
H1	IO_L42N_GCLK24_M3LDM_3	C_CLK_INH_B	3	2.5V
J3	IO_L43N_GCLK22_IRDY2_M3CASN_3	C_CLK_OSC	3	2.5V
R3	IO_L65N_CSO_B_2	C_CSO_B	2	2.5V
K1	IO_L40N_M3DQ7_3	C_DIPSW_0	3	2.5V
L1	IO_L39N_M3LDQSN_3	C_DIPSW_1	3	2.5V
L2	IO_L39P_M3LDQS_3	C_DIPSW_2	3	2.5V
M1	IO_L38N_M3DQ3_3	C_DIPSW_3	3	2.5V
N1	IO_L37N_M3DQ1_3	C_DIPSW_4	3	2.5V
N2	IO_L37P_M3DQ0_3	C_DIPSW_5	3	2.5V
P1	IO_L2N_3	C_DIPSW_6	3	2.5V
M3	IO_L38P_M3DQ2_3	C_DIPSW_7	3	2.5V
P15	IO_L74N_DOUT_BUSY_1	C_FTDI_RESET_B	1	2.5V
N4	IO_L63P_2	C_HEADER_0	2	2.5V
M5	IO_L64P_D8_2	C_HEADER_1	2	2.5V
N5	IO_L64N_D9_2	C_HEADER_2	2	2.5V
M6	IO_L47N_2	C_HEADER_3	2	2.5V
N6	IO_L48P_D7_2	C_HEADER_4	2	2.5V
R4	IO_L63N_2	C_HEADER_5	2	2.5V
P5	IO_L49P_D3_2	C_HEADER_6	2	2.5V
R5	IO_L49N_D4_2	C_HEADER_7	2	2.5V
R6	IO_L48N_RDWR_B_VREF_2	C_HEADER_8	2	2.5V
P7	IO_L32P_GCLK29_2	C_HEADER_9	2	2.5V
R7	IO_L32N_GCLK28_2	C_HEADER_10	2	2.5V
R8	IO_L29N_GCLK2_2	C_HEADER_11	2	2.5V
N8	IO_L29P_GCLK3_2	C_HEADER_12	2	2.5V
R9	IO_L16N_VREF_2	C_HEADER_13	2	2.5V
P9	IO_L16P_2	C_HEADER_14	2	2.5V
R10	IO_L13N_D10_2	C_HEADER_15	2	2.5V
L5	IO_L62N_D6_2	C_HEADER_16	2	2.5V

L6	IO_L62P_D5_2	C_HEADER_17	2	2.5V
L8	IO_L31N_GCLK30_D15_2	C_HEADER_18	2	2.5V
M9	IO_L15P_2	C_HEADER_19	2	2.5V
N9	IO_L15N_2	C_HEADER_20	2	2.5V
M10	IO_L14N_D12_2	C_HEADER_21	2	2.5V
N11	IO_L12N_D2_MISO3_2	C_HEADER_22	2	2.5V
M11	IO_L12P_D1_MISO2_2	C_HEADER_23	2	2.5V
N7	IO_L30N_GCLK0_USERCCLK_2	C_HEADER_CLK_N	2	2.5V
M8	IO_L30P_GCLK1_D13_2	C_HEADER_CLK_P	2	2.5V
B2	IO_L1P_HSWAPEN_0	C_HSWAPEN	0	2.5V
P3	IO_L65P_INIT_B_2	C_INIT_B	2	2.5V
F1	IO_L46N_M3CLKN_3	C_LED_0	3	2.5V
G2	IO_L44P_GCLK21_M3A5_3	C_LED_1	3	2.5V
G1	IO_L44N_GCLK20_M3A6_3	C_LED_2	3	2.5V
H3	IO_L42P_GCLK25_TRDY2_M3UDM_3	C_LED_3	3	2.5V
H4	IO_L47N_M3A1_3	C_LED_4	3	2.5V
H5	IO_L49N_M3A2_3	C_LED_5	3	2.5V
J5	IO_L47P_M3A0_3	C_LED_6	3	2.5V
J4	IO_L45N_M3ODT_3	C_LED_7	3	2.5V
K5	IO_L45P_M3A3_3	C_LED_8	3	2.5V
K4	IO_L43P_GCLK23_M3RASN_3	C_LED_9	3	2.5V
R12	IO_L1N_M0_CMPMISO_2	C_M0	2	2.5V
N10	IO_L13P_M1_2	C_M1	2	2.5V
P11	IO_L3P_D0_DIN_MISO_MISO1_2	C_MISO	2	2.5V
R11	IO_L3N_MOSI_CSI_B_MISO0_2	C_MOSI	2	2.5V
L3	IO_L1N_VREF_3	C_PUSHSW_0	3	2.5V
M4	IO_L1P_3	C_PUSHSW_1	3	2.5V
P2	IO_L2P_3	C_RESET_B	3	2.5V
N15	IO_L47N_LDC_M1DQ1_1	FTDI_ACBUS0_RXF_B	1	2.5V
M15	IO_L46N_FOE_B_M1DQ3_1	FTDI_ACBUS1_TXE_B	1	2.5V
¥L14	IO_L45P_A1_M1LDQS_1	FTDI_ACBUS2_RD_B	1	2.5V
L15	IO_L45N_A0_M1LDQSN_1	FTDI_ACBUS3_WR_B	1	2.5V
K15	IO_L44N_A2_M1DQ7_1	FTDI_ACBUS4_SIWUA	1	2.5V
J14	IO_L43P_GCLK5_M1DQ4_1	FTDI_ACBUS5_CLKOUT	1	2.5V
J13	IO_L36N_A8_M1BA1_1	FTDI_ACBUS6_OE_B	1	2.5V
J15	IO_L43N_GCLK4_M1DQ5_1	FTDI_ACBUS7	1	2.5V

M13	IO_L46P_FCS_B_M1DQ2_1	FTDI_ADBUS0	1	2.5V
L12	IO_L40N_GCLK10_M1A6_1	FTDI_ADBUS1	1	2.5V
K12	IO_L40P_GCLK11_M1A5_1	FTDI_ADBUS2	1	2.5V
K13	IO_L44P_A3_M1DQ6_1	FTDI_ADBUS3	1	2.5V
K11	IO_L38N_A4_M1CLKN_1	FTDI_ADBUS4	1	2.5V
J11	IO_L36P_A9_M1BA0_1	FTDI_ADBUS5	1	2.5V
H11	IO_L32N_A16_M1A9_1	FTDI_ADBUS6	1	2.5V
H12	IO_L34P_A13_M1WE_1	FTDI_ADBUS7	1	2.5V
P14	IO_L74P_AWAKE_1	FTDI_PWREN_B	1	2.5V
N14	IO_L47P_FWE_B_M1DQ0_1	FTDI_SUSPEND_B	1	2.5V
D1	IO_L54N_M3A11_3	MC_IC_D0	3	2.5V
C1	IO_L83N_VREF_3	MC_IC_D1	3	2.5V
C2	IO_L83P_3	MC_IC_D2	3	2.5V
B3	IO_L2P_0	MC_IC_D3	0	2.5V
A3	IO_L2N_0	MC_IC_D4	0	2.5V
A4	IO_L4N_0	MC_IC_D5	0	2.5V
B5	IO_L6P_0	MC_IC_D6	0	2.5V
A5	IO_L6N_0	MC_IC_D7	0	2.5V
B7	IO_L35P_GCLK17_0	MC_IC_D8	0	2.5V
A7	IO_L35N_GCLK16_0	MC_IC_D9	0	2.5V
A8	IO_L36N_GCLK14_0	MC_IC_D10	0	2.5V
A9	IO_L37N_GCLK12_0	MC_IC_D11	0	2.5V
B9	IO_L37P_GCLK13_0	MC_IC_D12	0	2.5V
A10	IO_L62N_VREF_0	MC_IC_D13	0	2.5V
A11	IO_L63N_SCP6_0	MC_IC_D14	0	2.5V
B11	IO_L63P_SCP7_0	MC_IC_D15	0	2.5V
A12	IO_L66N_SCP0_0	MC_IC_D16	0	2.5V
A13	IO_L65N_SCP2_0	MC_IC_D17	0	2.5V
B13	IO_L65P_SCP3_0	MC_IC_D18	0	2.5V
B15	IO_L1N_A24_VREF_1	MC_IC_D19	1	2.5V
C14	IO_L33P_A15_M1A10_1	MC_IC_D20	1	2.5V
C15	IO_L33N_A14_M1A4_1	MC_IC_D21	1	2.5V
D15	IO_L35N_A10_M1A2_1	MC_IC_D22	1	2.5V
E14	IO_L37P_A7_M1A0_1	MC_IC_D23	1	2.5V
E15	IO_L37N_A6_M1A1_1	MC_IC_D24	1	2.5V
F15	IO_L39N_M1ODT_1	MC_IC_D25	1	2.5V

G14	IO_L41P_GCLK9_IRDY1_M1RASN_1	MC_IC_D26	1	2.5V
G15	IO_L41N_GCLK8_M1CASN_1	MC_IC_D27	1	2.5V
H15	IO_L42N_GCLK6_TRDY1_M1LDM_1	MC_IC_D28	1	2.5V
G3	IO_L48N_M3BA1_3	MC_IC_D29	3	2.5V
F4	IO_L50N_M3BA2_3	MC_IC_D30	3	2.5V
F3	IO_L46P_M3CLK_3	MC_IC_D31	3	2.5V
F5	IO_L50P_M3WE_3	MC_IC_D32	3	2.5V
E3	IO_L53N_M3A12_3	MC_IC_D33	3	2.5V
D5	IO_L3P_0	MC_IC_D34	0	2.5V
C5	IO_L3N_0	MC_IC_D35	0	2.5V
E6	IO_L5P_0	MC_IC_D36	0	2.5V
D7	IO_L7P_0	MC_IC_D37	0	2.5V
C8	IO_L36P_GCLK15_0	MC_IC_D38	0	2.5V
D8	IO_L34N_GCLK18_0	MC_IC_D39	0	2.5V
E7	IO_L34P_GCLK19_0	MC_IC_D40	0	2.5V
E8	IO_L38N_VREF_0	MC_IC_D41	0	2.5V
E9	IO_L40N_0	MC_IC_D42	0	2.5V
D10	IO_L39P_0	MC_IC_D43	0	2.5V
C10	IO_L62P_0	MC_IC_D44	0	2.5V
C11	IO_L64N_SCP4_0	MC_IC_D45	0	2.5V
D11	IO_L64P_SCP5_0	MC_IC_D46	0	2.5V
C12	IO_L66P_SCP1_0	MC_IC_D47	0	2.5V
G12	IO_L30N_A20_M1A11_1	MC_IC_D48	1	2.5V
D13	IO_L35P_A11_M1A7_1	MC_IC_D49	1	2.5V
F12	IO_L31N_A18_M1A12_1	MC_IC_D50	1	2.5V
H13	IO_L42P_GCLK7_M1UDM_1	M_CCLK_R	1	2.5V
A6	IO_L33N_0	M_CSO_B_R	0	2.5V
G13	IO_L34N_A12_M1BA2_1	M_D0_DIN_MISO_R	1	2.5V
C9	IO_L39N_0	M_D1_R	0	2.5V
F11	IO_L31P_A19_M1CKE_1	M_D2_R	1	2.5V
C4	IO_L4P_0	M_D3_R	0	2.5V
C6	IO_L33P_0	M_D4_R	0	2.5V
D3	IO_L54P_M3RESET_3	M_D5_R	3	2.5V
D4	IO_L53P_M3CKE_3	M_D6_R	3	2.5V
D6	IO_L5N_0	M_D7_R	0	2.5V
F13	IO_L39P_M1A3_1	M_DONE_R	1	2.5V

G11	IO_L30P_A21_M1RESET_1	M_DOUT_BUSY_R	1	2.5V
E4	IO_L51N_M3A4_3	M_INIT_B_R	3	2.5V
E2	IO_L52P_M3A8_3	M_M0_REMOTE	3	2.5V
E1	IO_L52N_M3A9_3	M_M1_REMOTE	3	2.5V
B14	IO_L1P_A25_1	M_MOSI_CSI_B_R	1	2.5V
A2	IO_L1N_VREF_0	M_PROG_B_R	0	2.5V
C7	IO_L7N_0	M_RDWR_B_R	0	2.5V

3.2.1. Clock and Reset

Table 41 : Controller FPGA (U2) Clock and Reset

Net	Pin (U2)	Destination	Voltage
C_CLK_OSC	J3	U14.OUT	2.5V
C_CLK_INH_B	H1	U14./INH	2.5V
C_CLK_EXT0_P	J2	J6	2.5V
C_CLK_EXT0_N	J1	J7	2.5V
C_RESET_B	P2	U15./RST	2.5V

3.2.2. User LED

Table 42 : Controller FPGA (U2) User LED

Net	Pin (U2)	Destination	Voltage
C_LED_0	F1	LED11	2.5V
C_LED_1	G2	LED12	2.5V
C_LED_2	G1	LED13	2.5V
C_LED_3	H3	LED14	2.5V
C_LED_4	H4	LED15	2.5V
C_LED_5	H5	LED16	2.5V
C_LED_6	J5	LED17	2.5V
C_LED_7	J4	LED18	2.5V
C_LED_8	K5	LED19	2.5V
C_LED_9	K4	LED20	2.5V

3.2.3. User Push switch

Table 43 : Controller FPGA (U2) User Push switch

Net	Pin (U2)	Destination	Voltage
C_PUSHSW_0	L3	SW8	2.5V
C_PUSHSW_1	M4	SW9	2.5V

3.2.4. User DIP switch

Table 44 : Controller FPGA (U2) User DIP switch

Net	Pin (U2)	Destination	Voltage
C_DIPSW_0	K1	SW10.1	2.5V
C_DIPSW_1	L1	SW10.2	2.5V
C_DIPSW_2	L2	SW10.3	2.5V
C_DIPSW_3	M1	SW10.4	2.5V
C_DIPSW_4	N1	SW10.5	2.5V
C_DIPSW_5	N2	SW10.6	2.5V
C_DIPSW_6	P1	SW10.7	2.5V
C_DIPSW_7	M3	SW10.8	2.5V

3.2.5. User Header

Table 45 : Controller FPGA (U2) User Header

Net	Pin (U2)	Destination	Voltage
C_HEADER_0	N4	CN5.1	2.5V
C_HEADER_1	M5	CN5.2	2.5V
C_HEADER_2	N5	CN5.3	2.5V
C_HEADER_3	M6	CN5.4	2.5V
C_HEADER_4	N6	CN5.5	2.5V
C_HEADER_5	R4	CN5.6	2.5V
C_HEADER_6	P5	CN5.7	2.5V
C_HEADER_7	R5	CN5.8	2.5V
C_HEADER_8	R6	CN5.11	2.5V
C_HEADER_9	P7	CN5.12	2.5V
C_HEADER_10	R7	CN5.13	2.5V
C_HEADER_11	R8	CN5.14	2.5V
C_HEADER_12	N8	CN5.15	2.5V
C_HEADER_13	R9	CN5.16	2.5V
C_HEADER_14	P9	CN5.17	2.5V
C_HEADER_15	R10	CN5.18	2.5V
C_HEADER_16	L5	CN5.21	2.5V
C_HEADER_17	L6	CN5.22	2.5V
C_HEADER_18	L8	CN5.23	2.5V
C_HEADER_19	M9	CN5.24	2.5V

C_HEADER_20	N9	CN5.25	2.5V
C_HEADER_21	M10	CN5.26	2.5V
C_HEADER_22	N11	CN5.27	2.5V
C_HEADER_23	M11	CN5.28	2.5V
C_HEADER_CLK_P	M8	CN5.31	2.5V
C_HEADER_CLK_N	N7	CN5.32	2.5V

3.2.6. USB Interface

Table 46 : Controller FPGA (U2) USB Interface

Net	Pin (U2)	Destination	Voltage
FTDI_ACBUS0_RXF_B	N15	U17.ACBUS0	2.5V
FTDI_ACBUS1_TXE_B	M15	U17.ACBUS1	2.5V
FTDI_ACBUS2_RD_B	¥L14	U17.ACBUS2	2.5V
FTDI_ACBUS3_WR_B	L15	U17.ACBUS3	2.5V
FTDI_ACBUS4_SIWUA	K15	U17.ACBUS4	2.5V
FTDI_ACBUS5_CLKOUT	J14	U17.ACBUS5	2.5V
FTDI_ACBUS6_OE_B	J13	U17.ACBUS6	2.5V
FTDI_ACBUS7	J15	U17.ACBUS7	2.5V
FTDI_ADBUS0	M13	U17.ADBUS0	2.5V
FTDI_ADBUS1	L12	U17.ADBUS1	2.5V
FTDI_ADBUS2	K12	U17.ADBUS2	2.5V
FTDI_ADBUS3	K13	U17.ADBUS3	2.5V
FTDI_ADBUS4	K11	U17.ADBUS4	2.5V
FTDI_ADBUS5	J11	U17.ADBUS5	2.5V
FTDI_ADBUS6	H11	U17.ADBUS6	2.5V
FTDI_ADBUS7	H12	U17.ADBUS7	2.5V
FTDI_PWREN_B	P14	U17.PWREN#	2.5V
FTDI_SUSPEND_B	N14	U17.SUSPEND#	2.5V
C_FTDI_RESET_B	P15	R120, JP6	2.5V

3.2.7. FPGA Interconnect

See Table 37.

3.2.8. Main FPGA Configuration

See Table 38.

3.2.9. Controller FPGA Configuration

Table 47 : Controller FPGA (U2) Configuration

Net	Pin (U2)	Destination	Voltage
C_CCLK	N12	U13.SCK	2.5V
C_CSO_B	R3	U13./CS	2.5V
C_DONE	R14	U15.RSTIN	2.5V
C_HSWAPEN	B2	R77 (Pull-down)	2.5V
C_INIT_B	P3	LED26	2.5V
C_M0	R12	R93 (Pull-up)	2.5V
C_M1	N10	R94 (Pull-down)	2.5V
C_MISO	P11	U13.SO	2.5V
C_MOSI	R11	U13.SI	2.5V
C_PROG_B	R2	SW11	2.5V

4. Board Design

4.1. Board Revision

The board revision is printed as “SAKURA-G-R1”, which means revision “R1” of SAKURA-G.

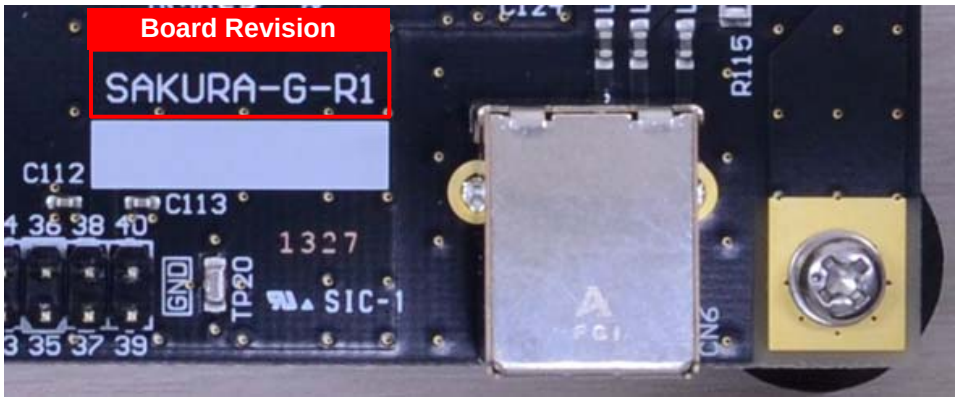


Figure 15 : Revision Mark

4.2. Schematic

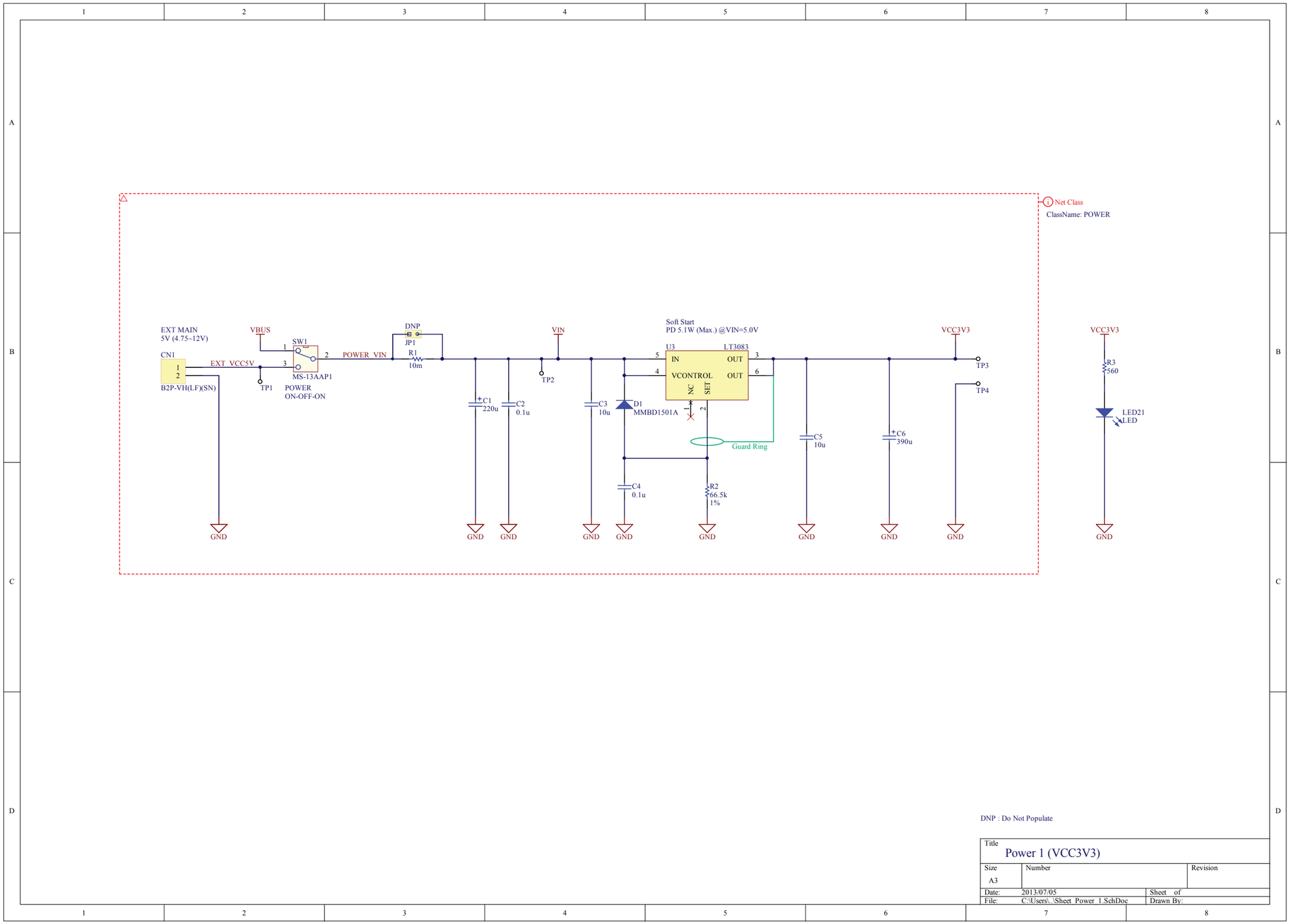


Figure 16 : Schematic – Power 1 (VCC3V3)

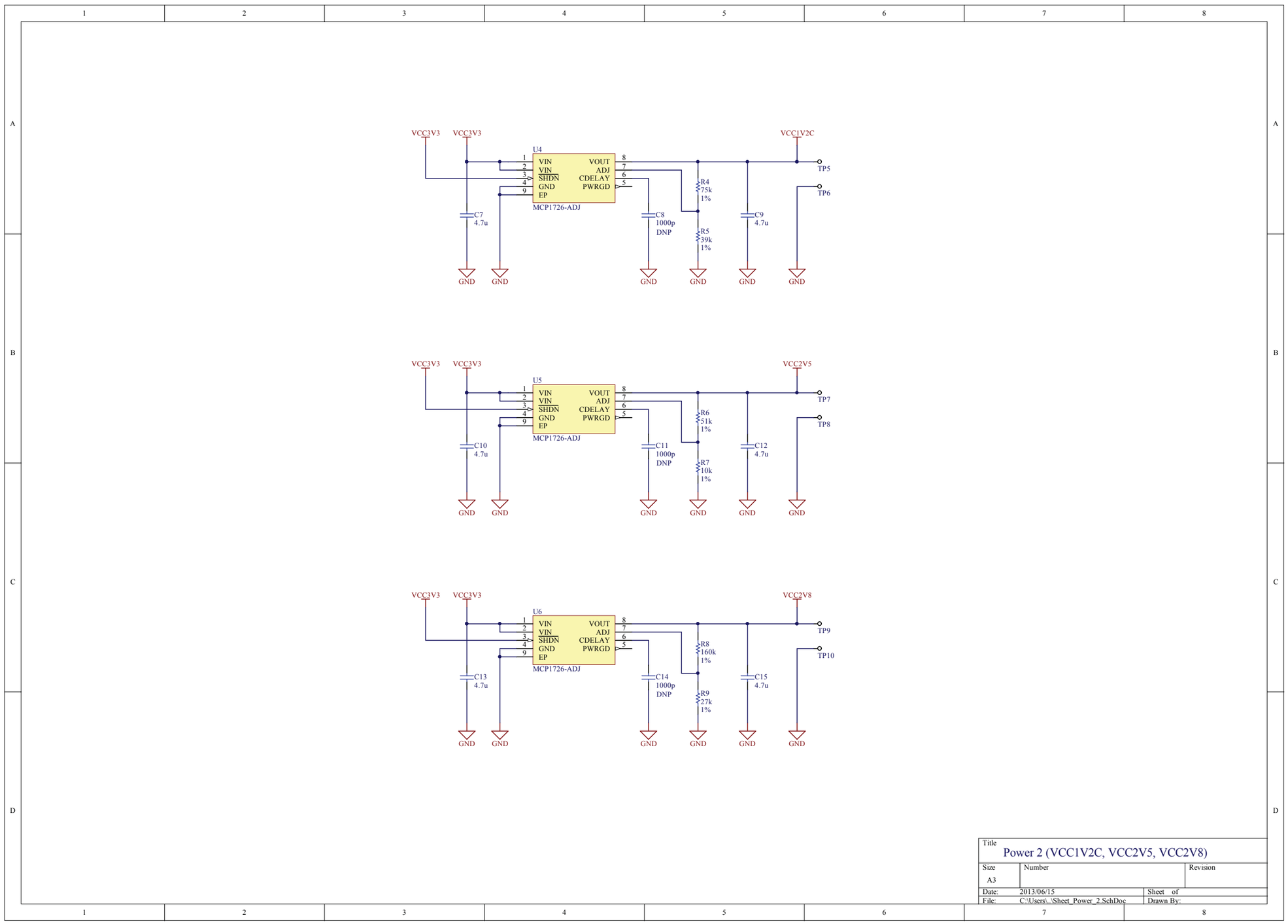


Figure 17 : Schematic – Power 2 (VCC1V2C, VCC2V5, VCC2V8)

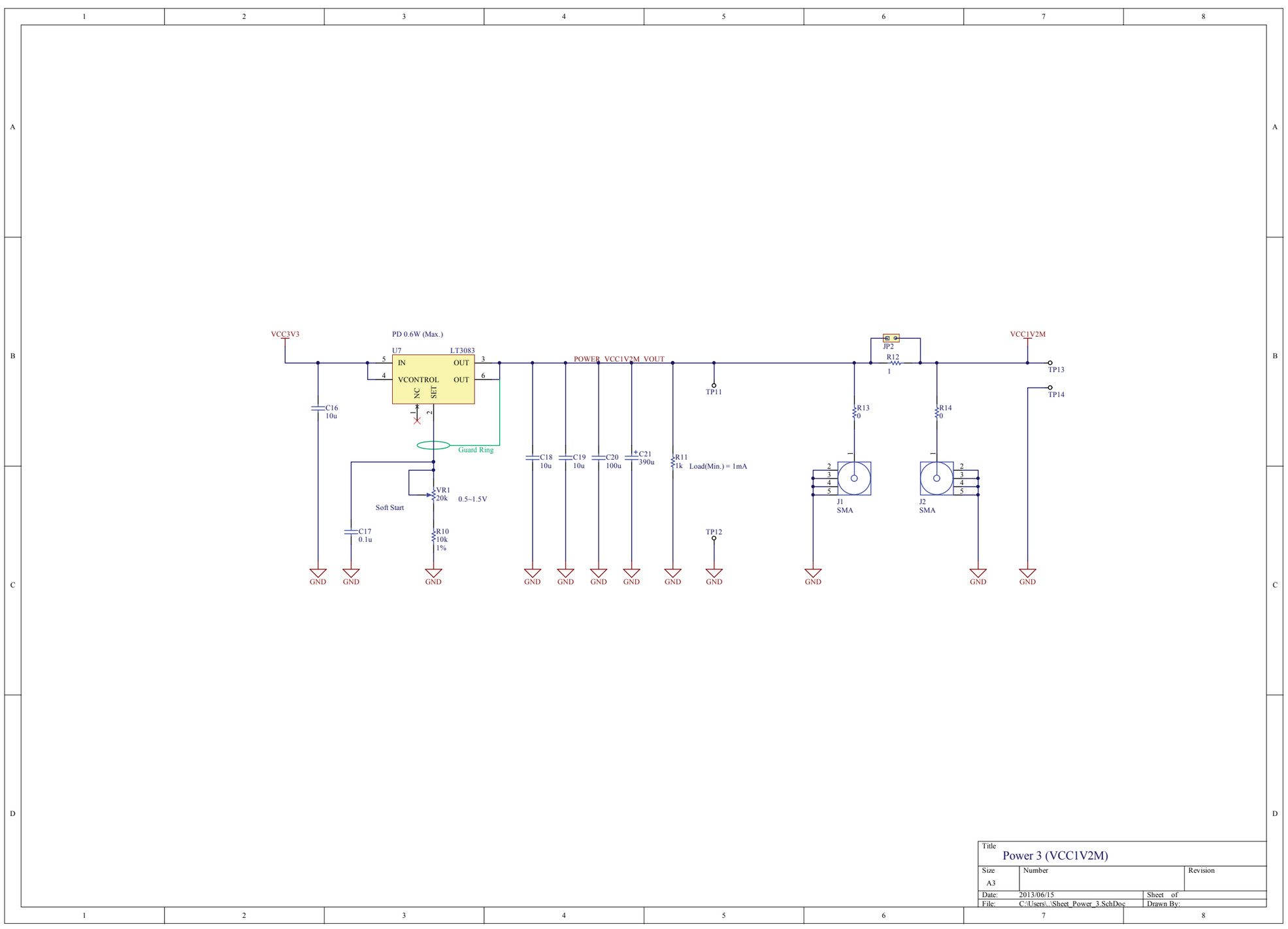


Figure 18 : Schematic – Power 3 (VCC1V2M)

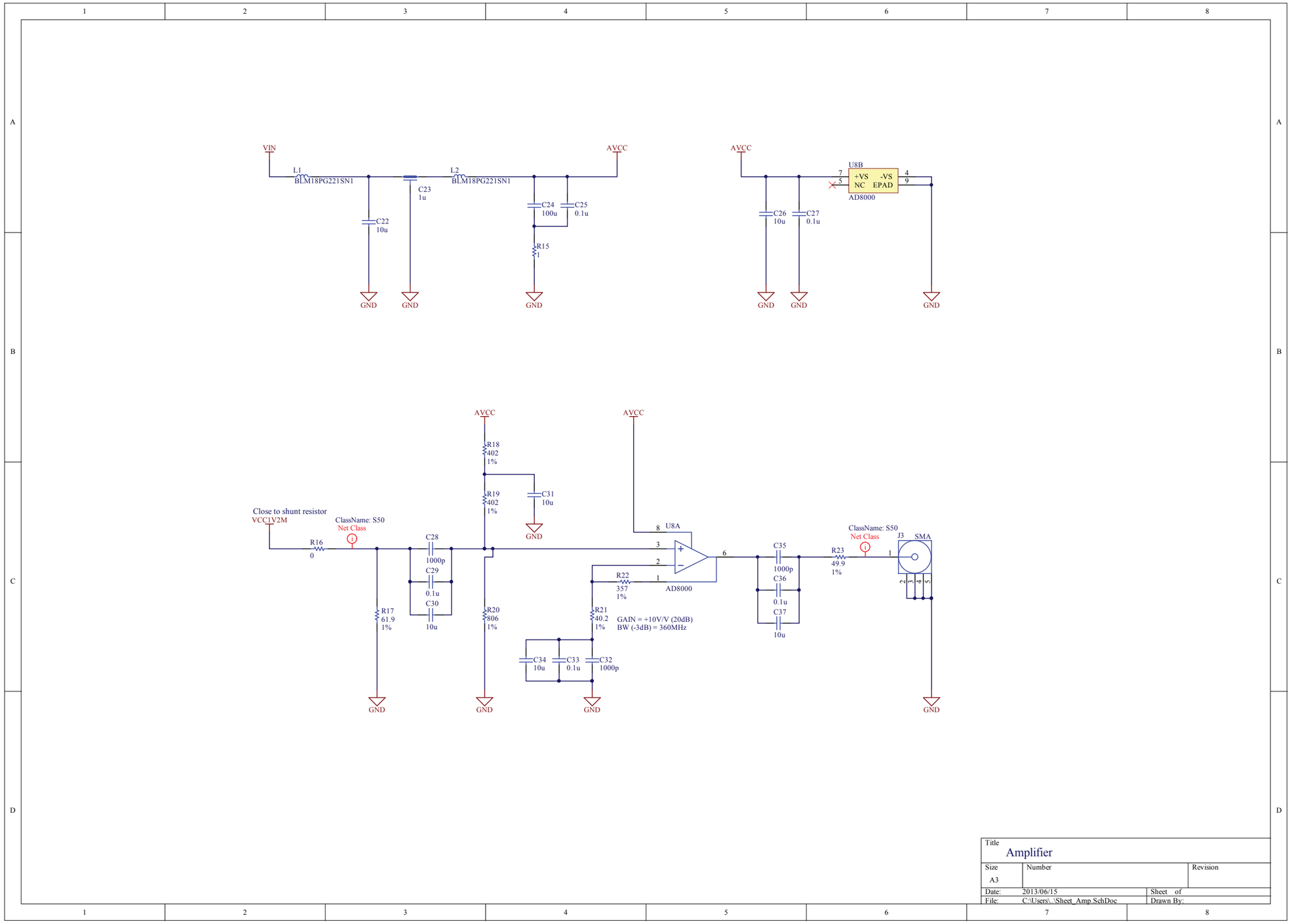


Figure 19 : Schematic – Amplifier

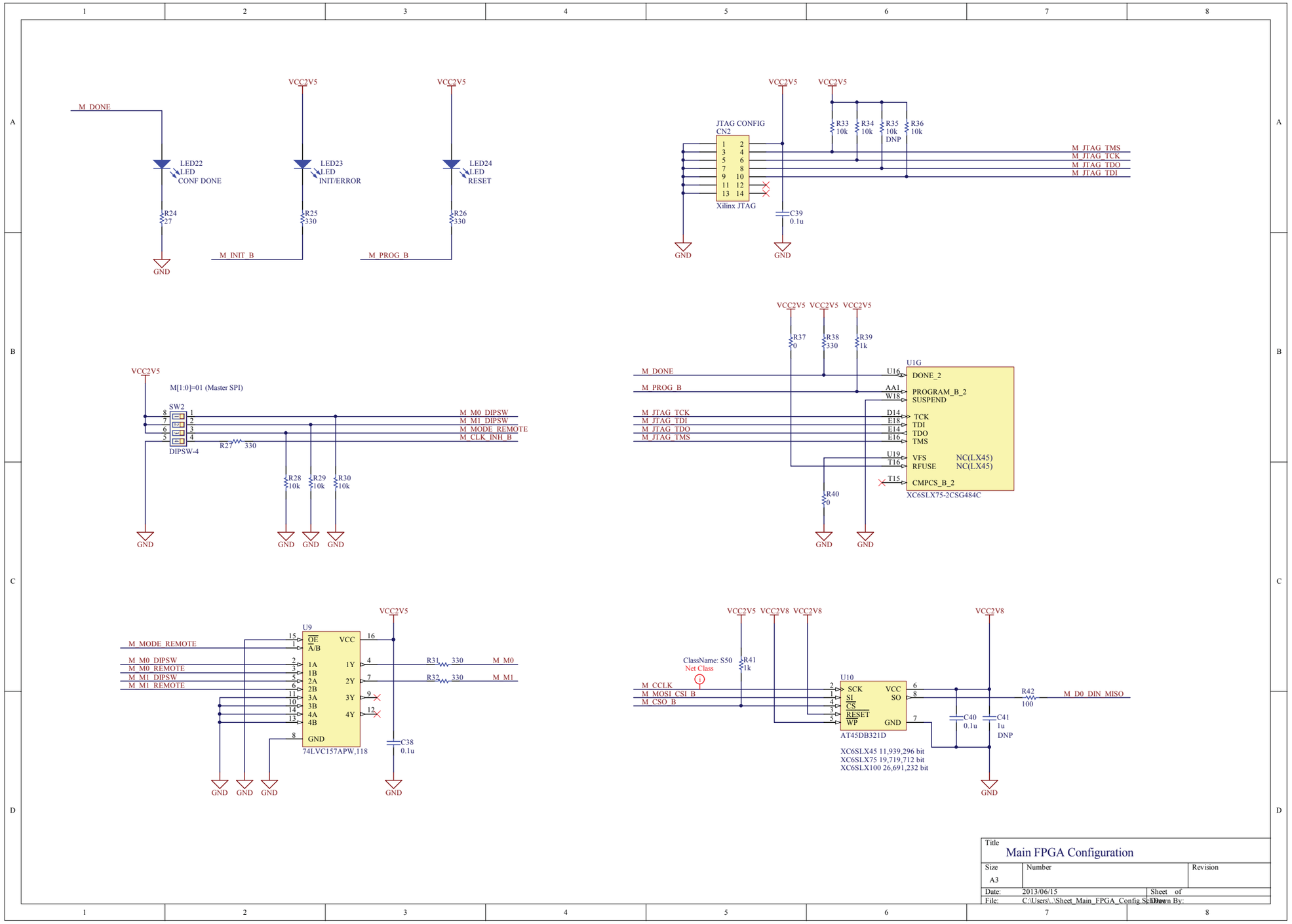


Figure 20 : Schematic – Main FPGA Configuration

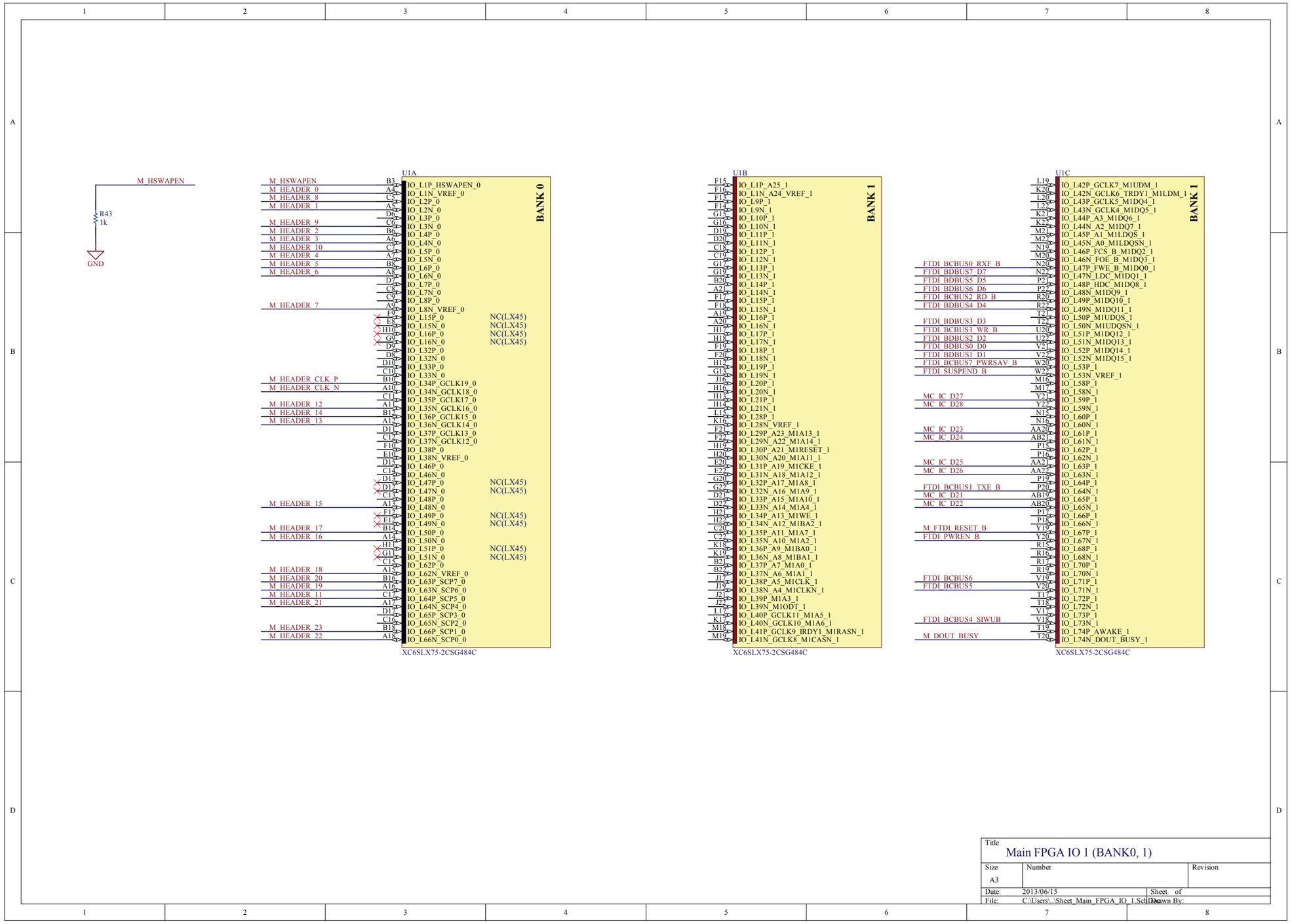


Figure 21 : Schematic – Main FPGA I/O (Bank 0, 1)

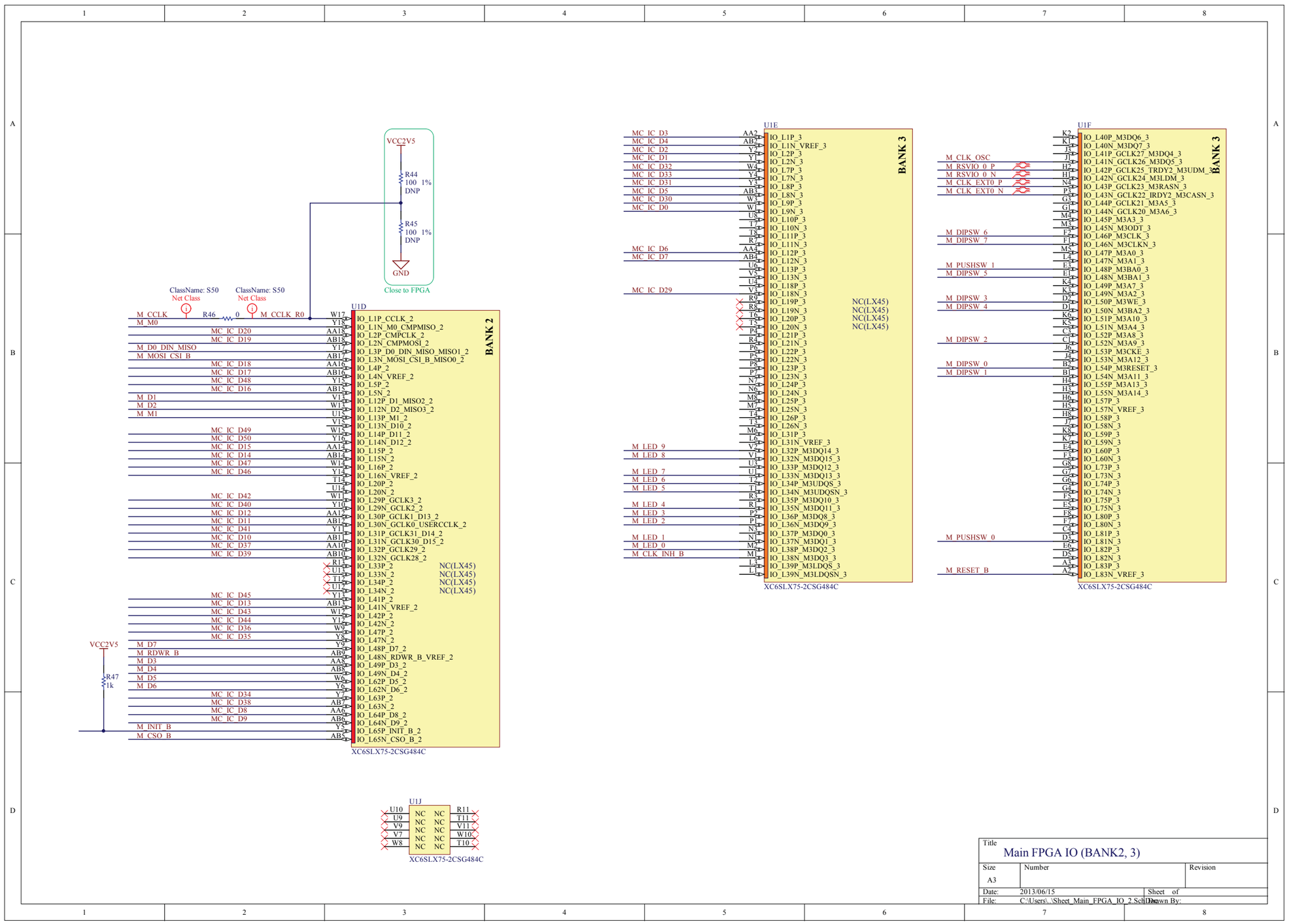


Figure 22 : Schematic – Main FPGA I/O (Bank 2, 3)

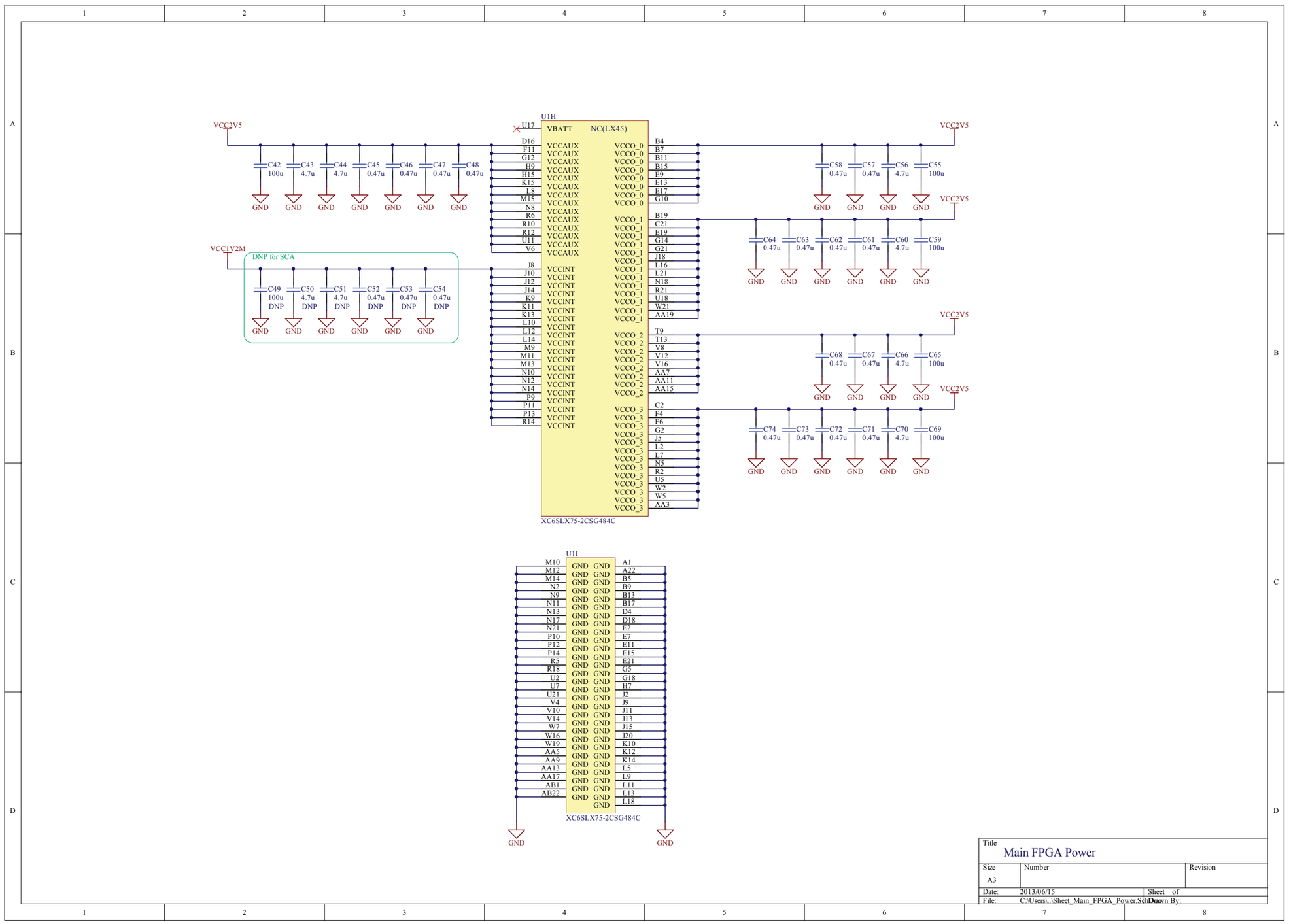


Figure 23 : Schematic – Main FPGA Power

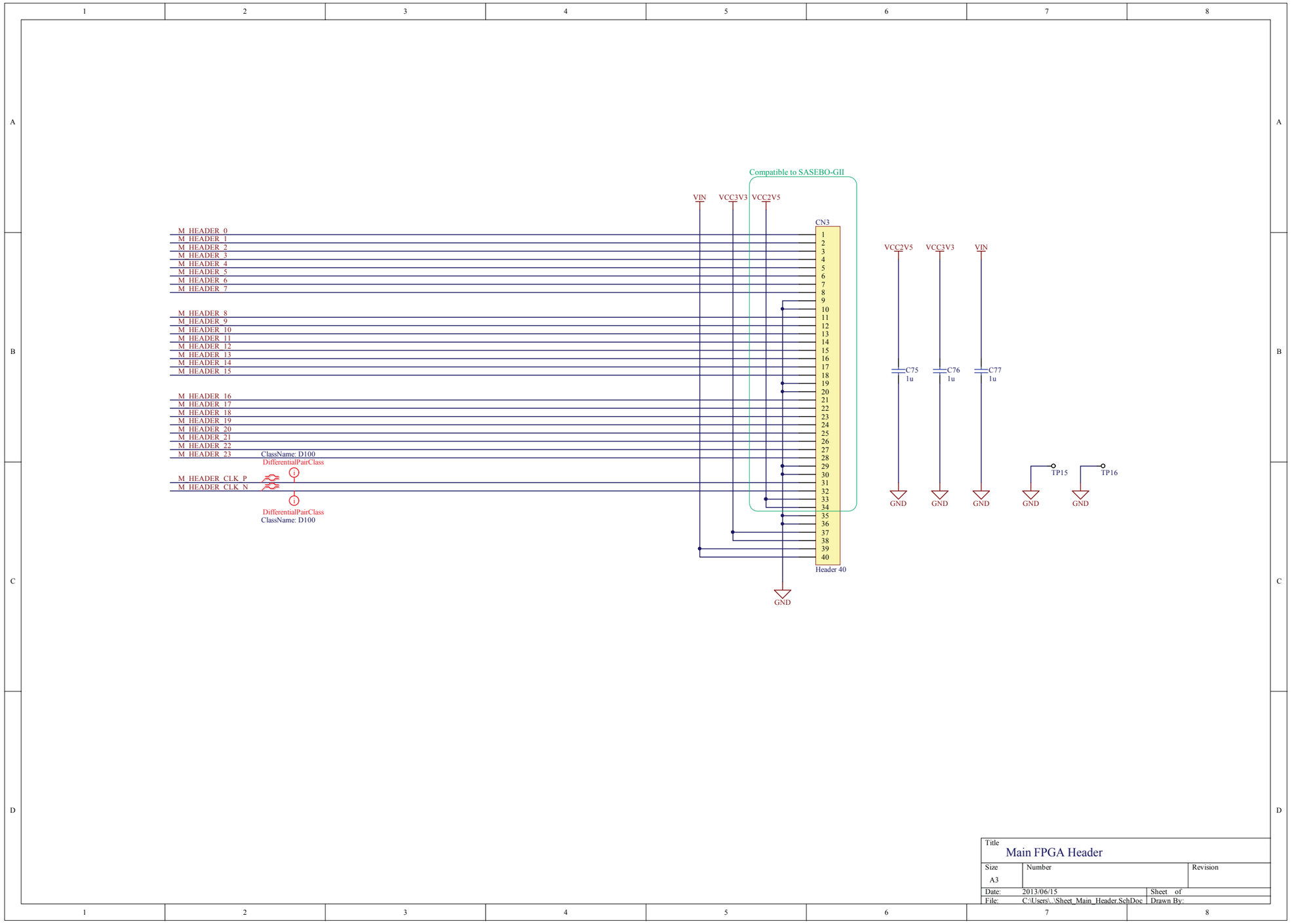


Figure 24 : Schematic – Main FPGA Header

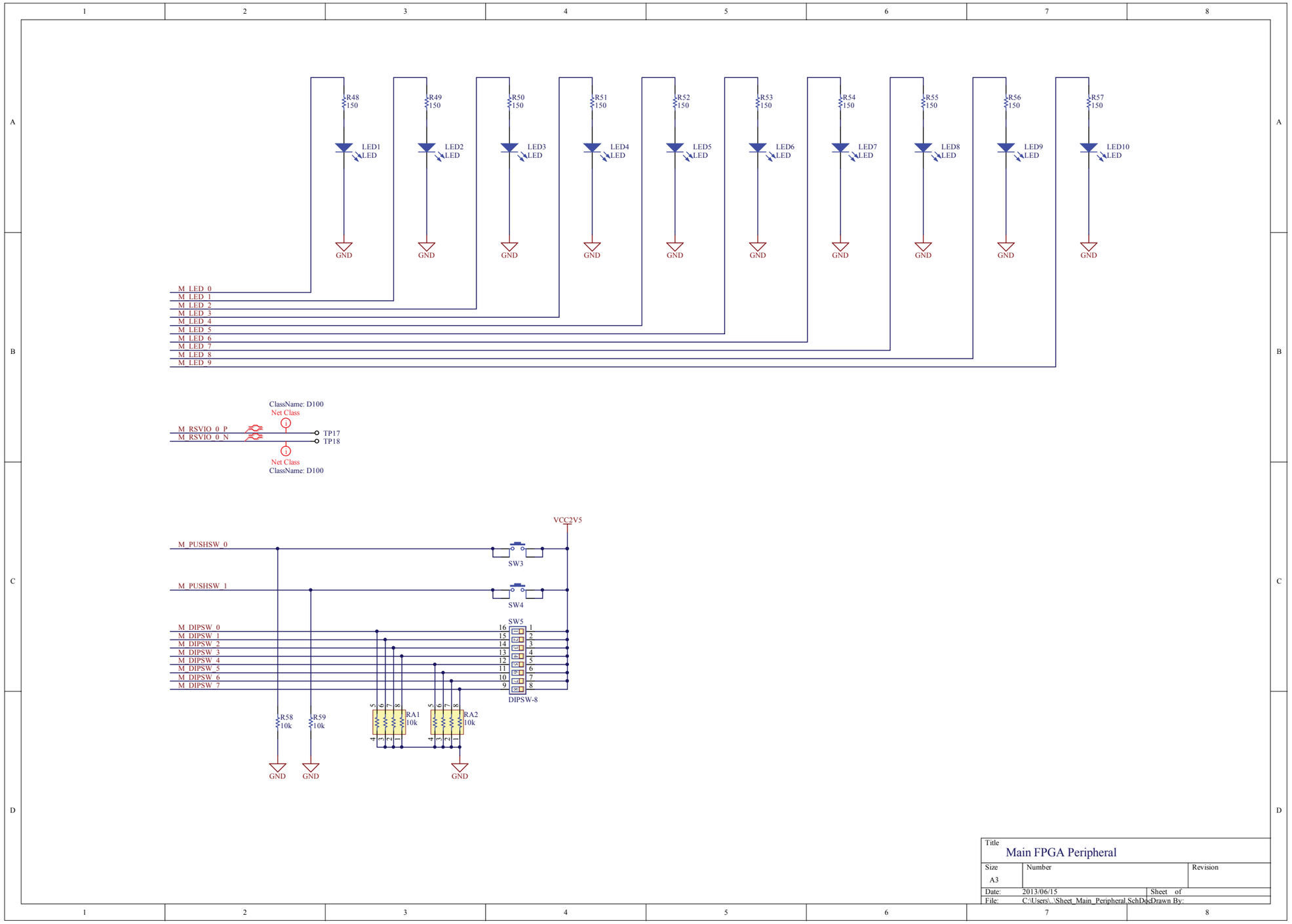


Figure 25 : Schematic – Main FPGA Peripheral

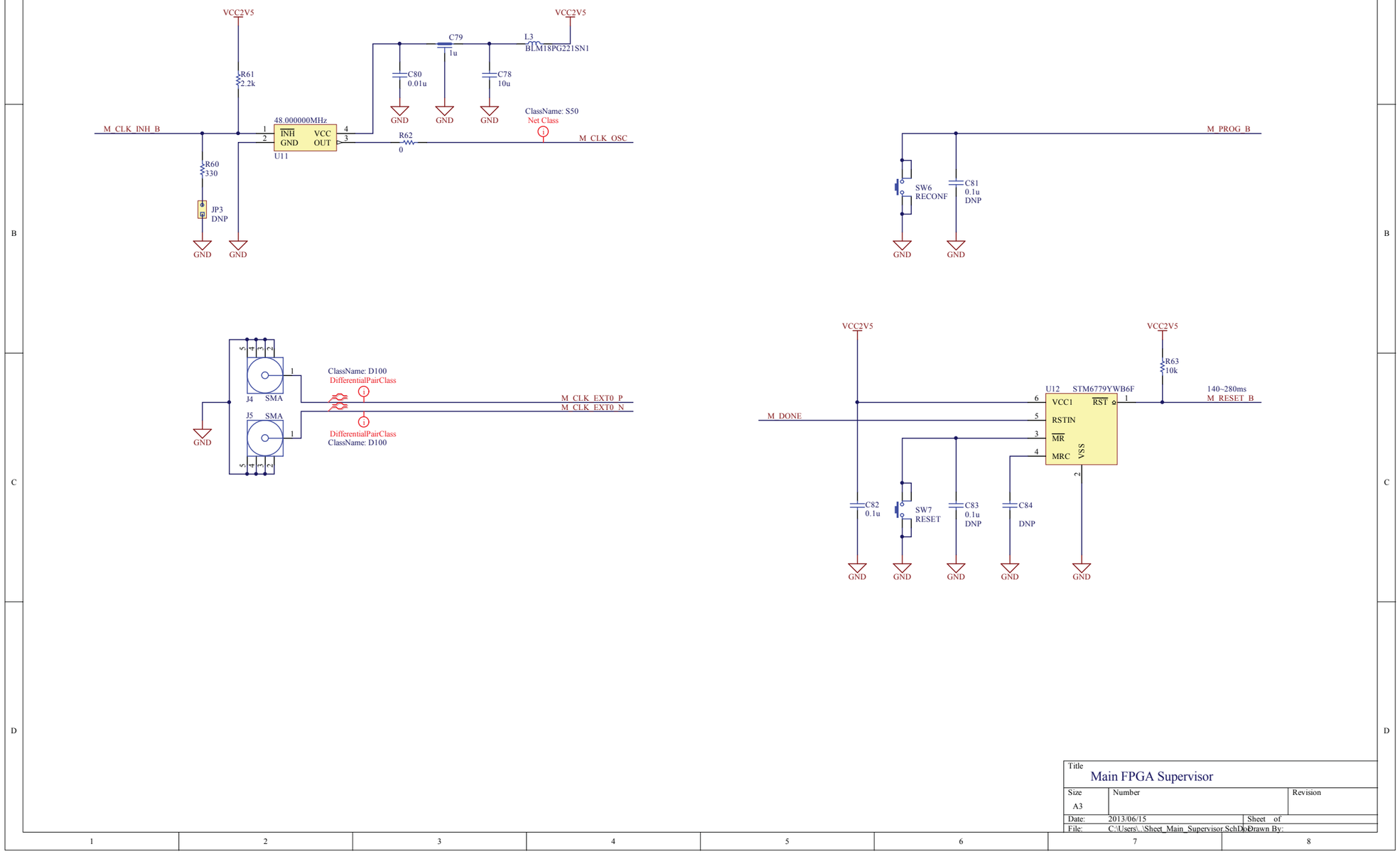


Figure 26 : Schematic – Main FPGA Supervisor

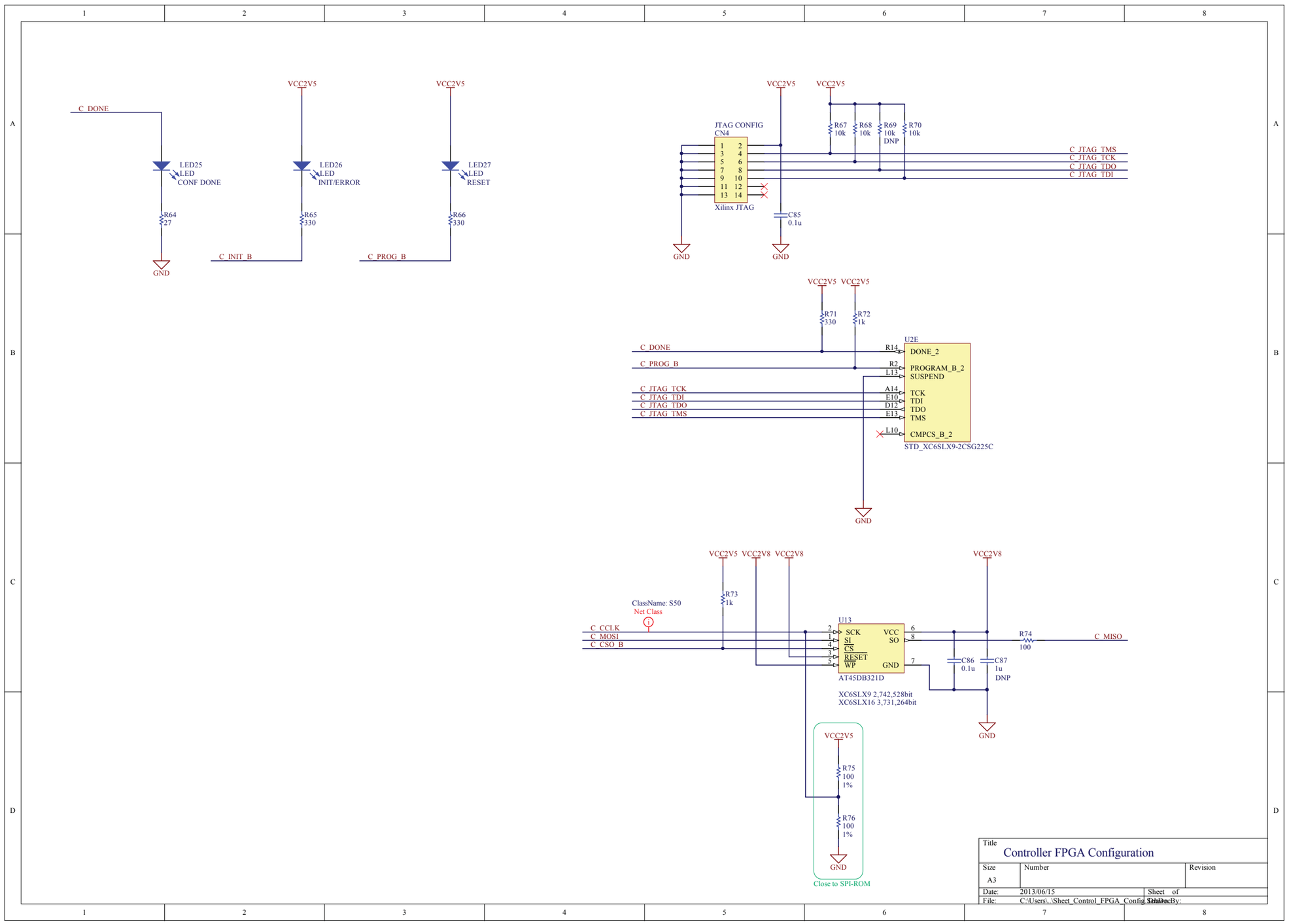


Figure 27 : Schematic – Main FPGA Configuration

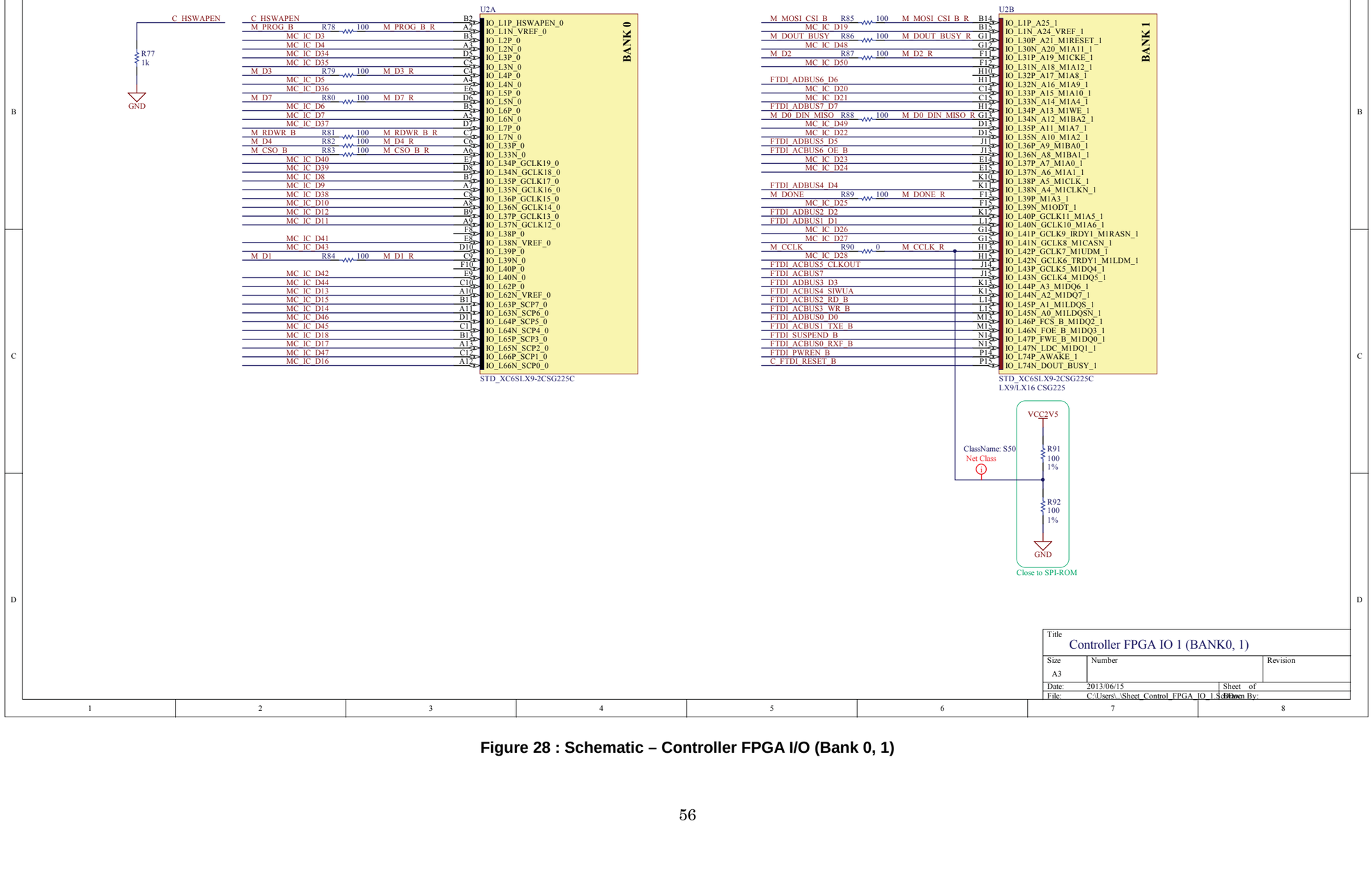


Figure 28 : Schematic – Controller FPGA I/O (Bank 0, 1)

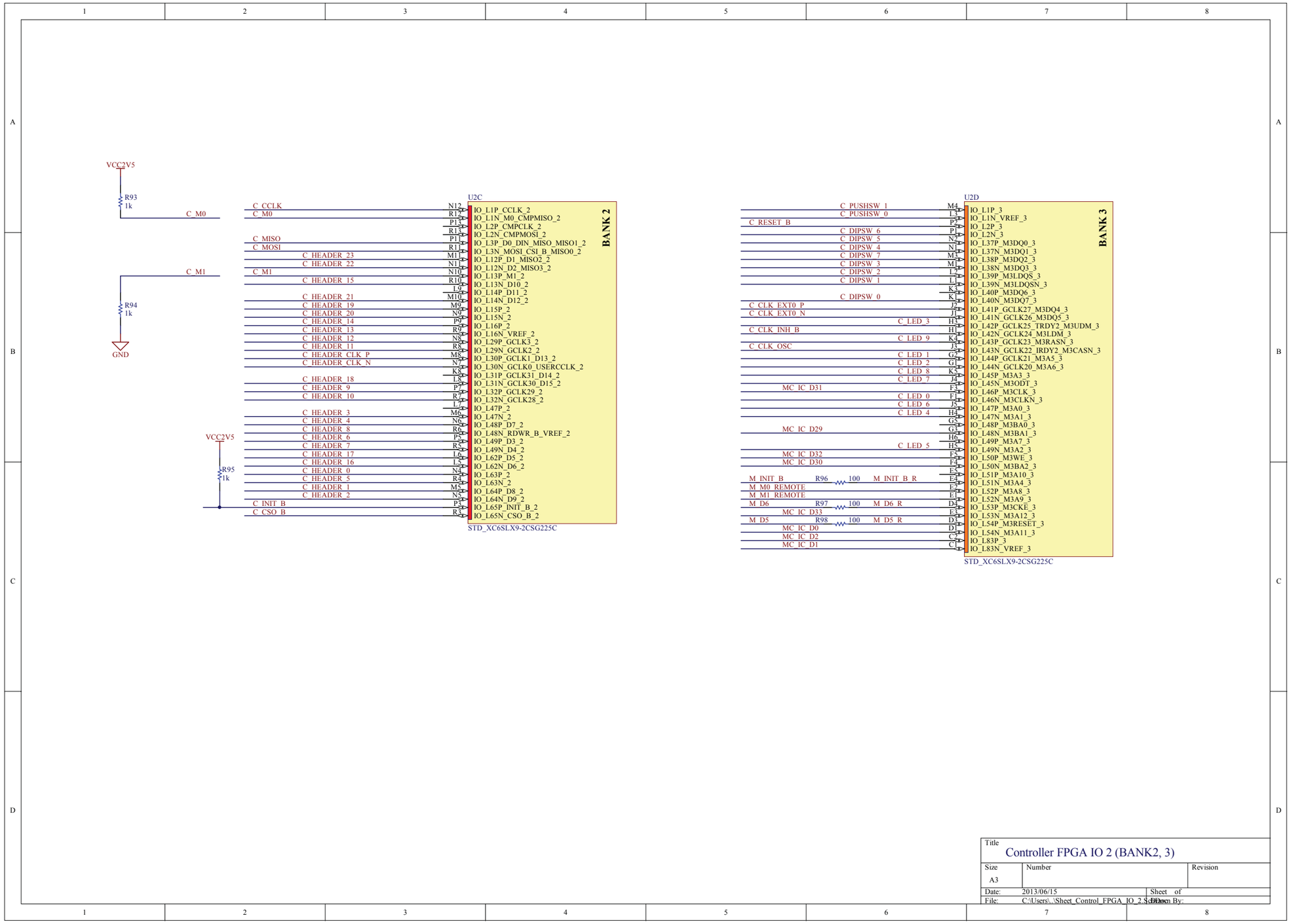


Figure 29 : Schematic – Controller FPGA I/O (Bank 2, 3)

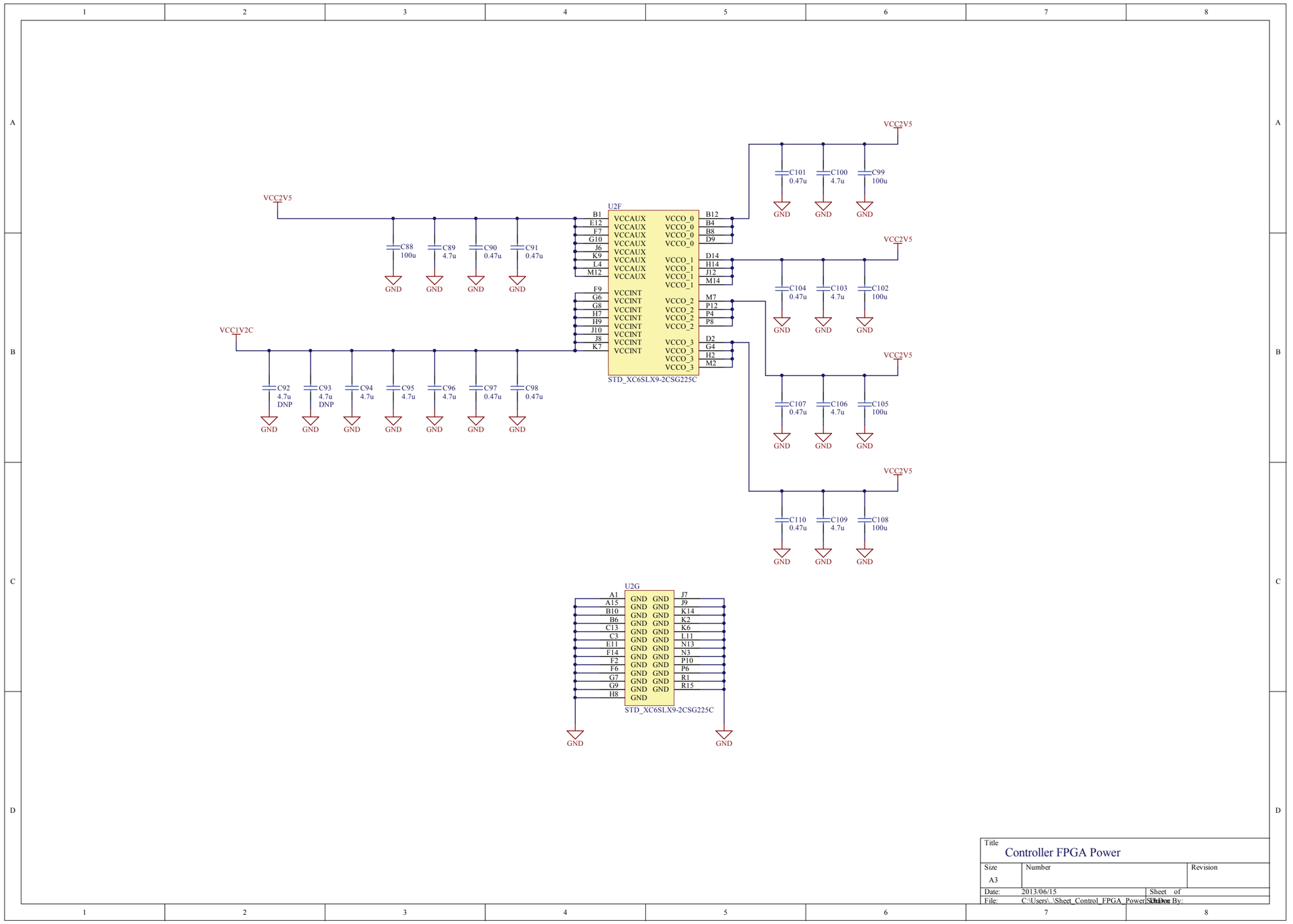


Figure 30 : Schematic – Controller FPGA Power

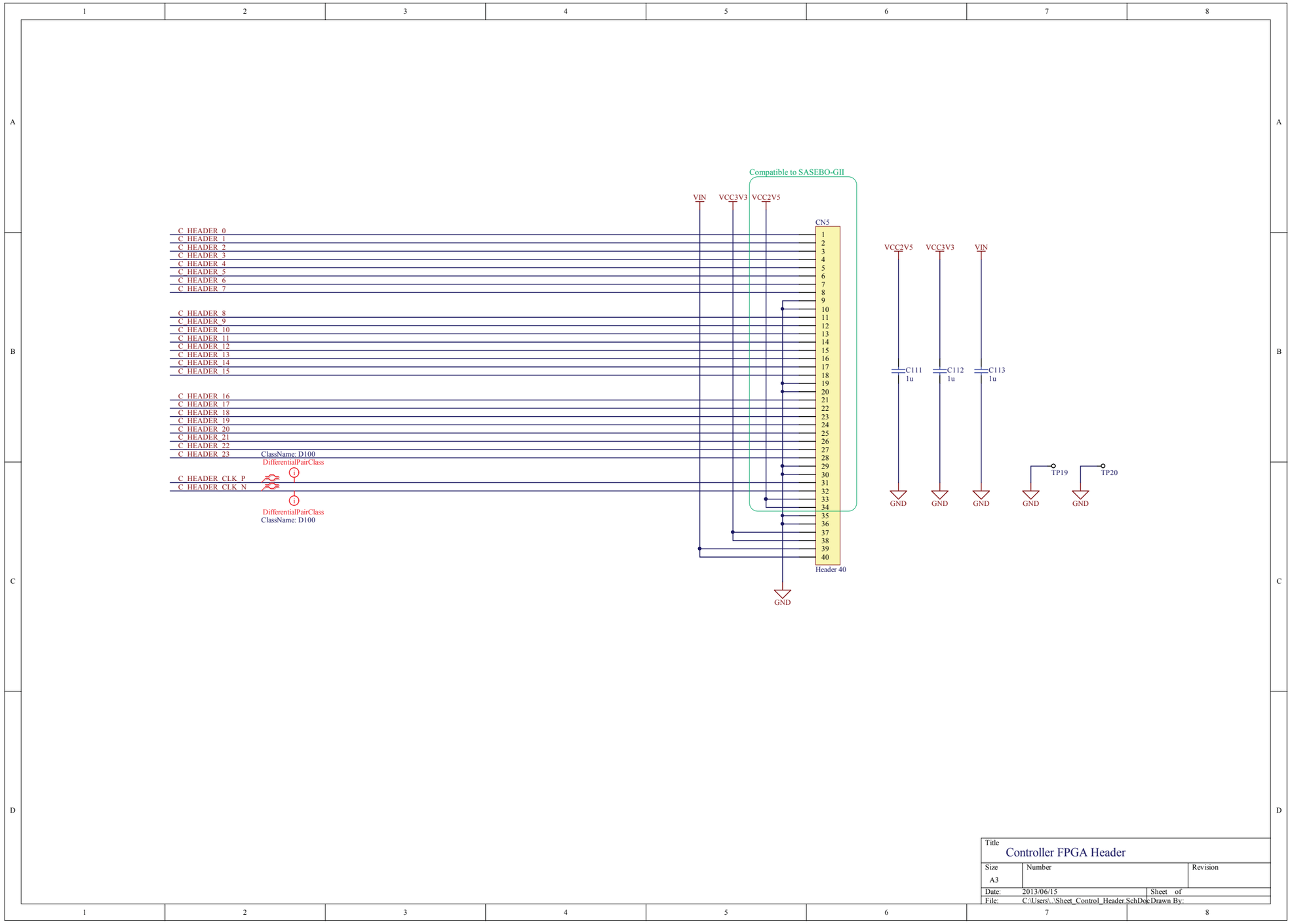


Figure 31 : Schematic – Controller FPGA Header

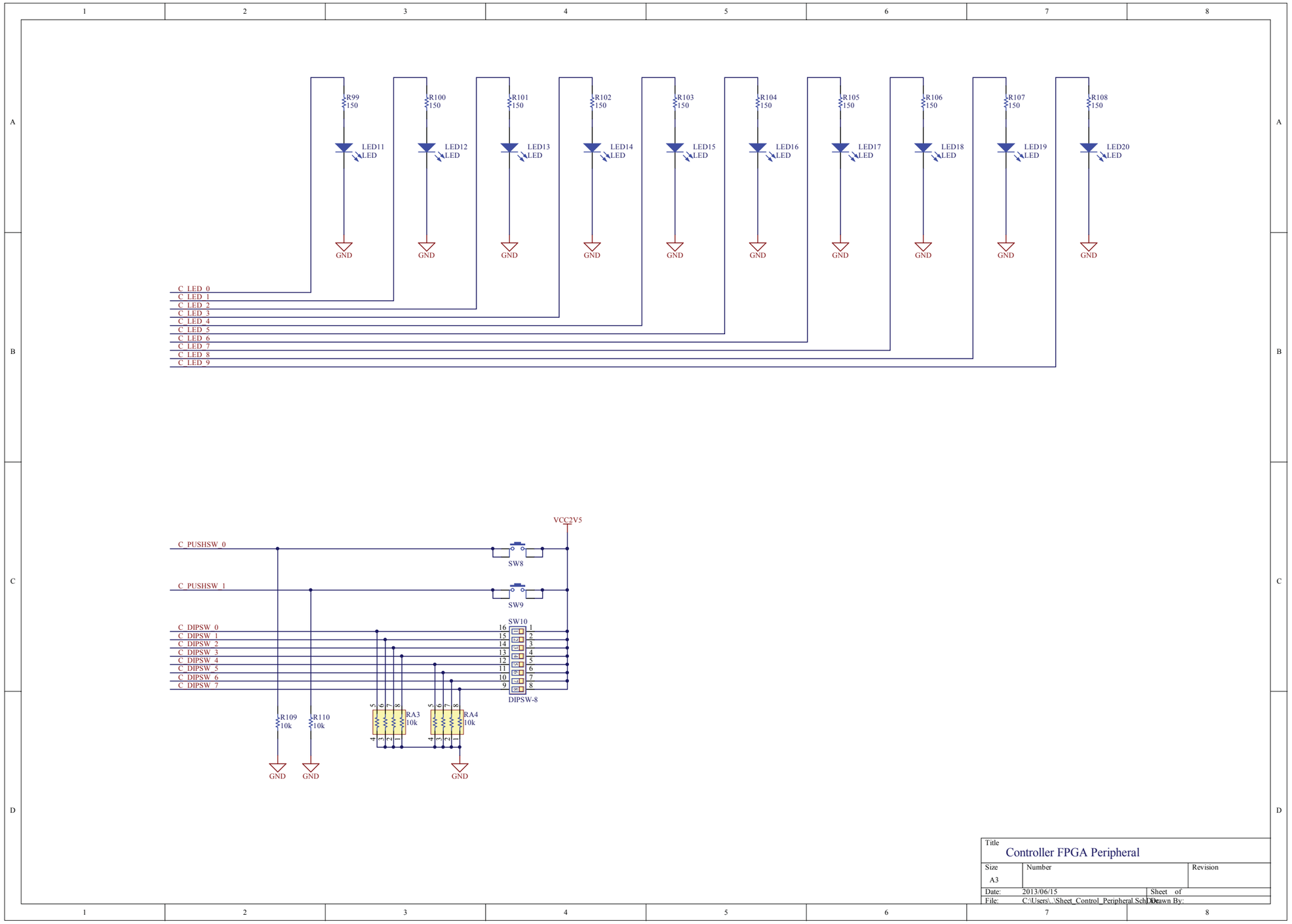


Figure 32 : Schematic – Controller FPGA Peripheral

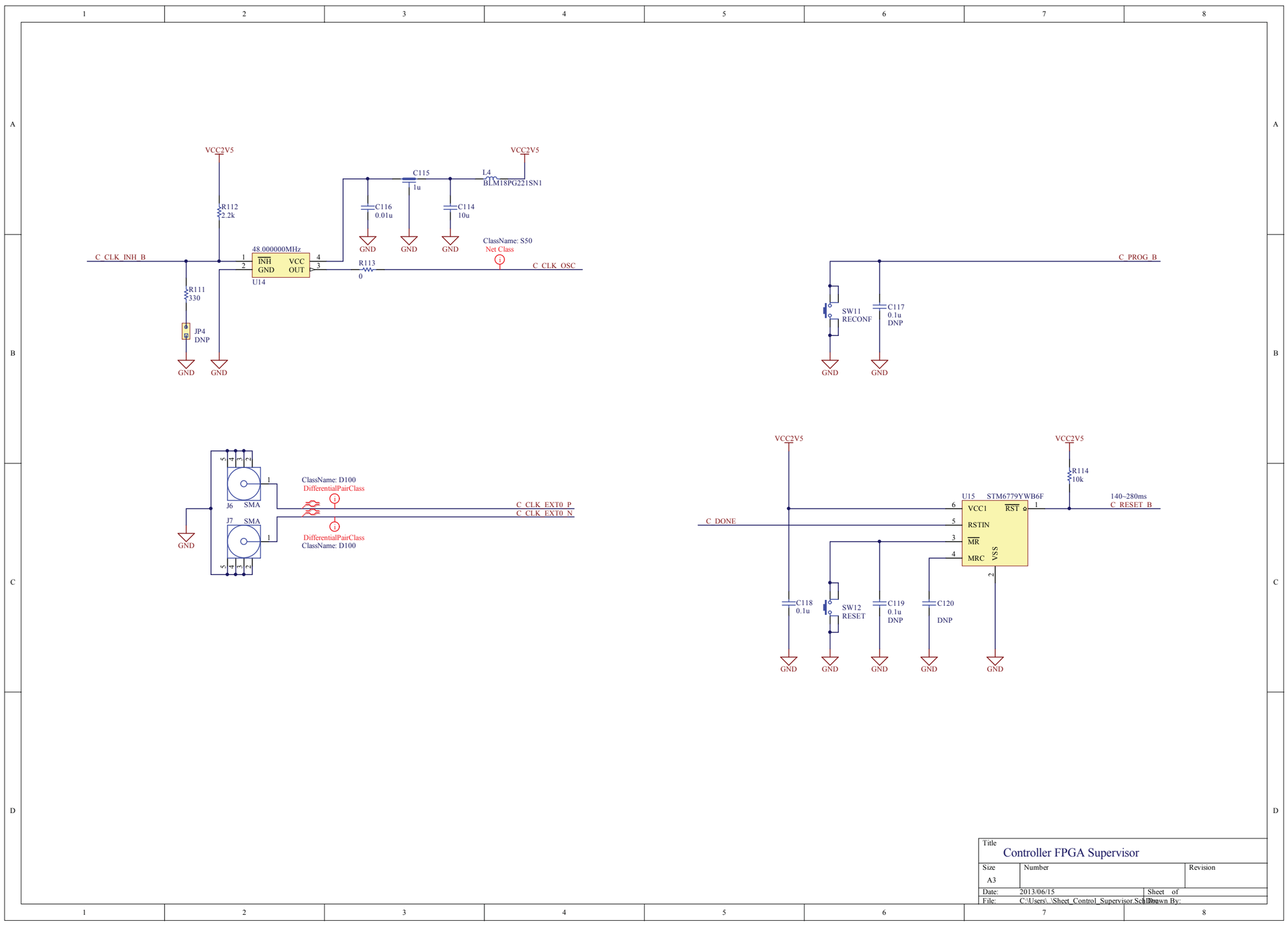


Figure 33 : Schematic – Controller FPGA Supervisor

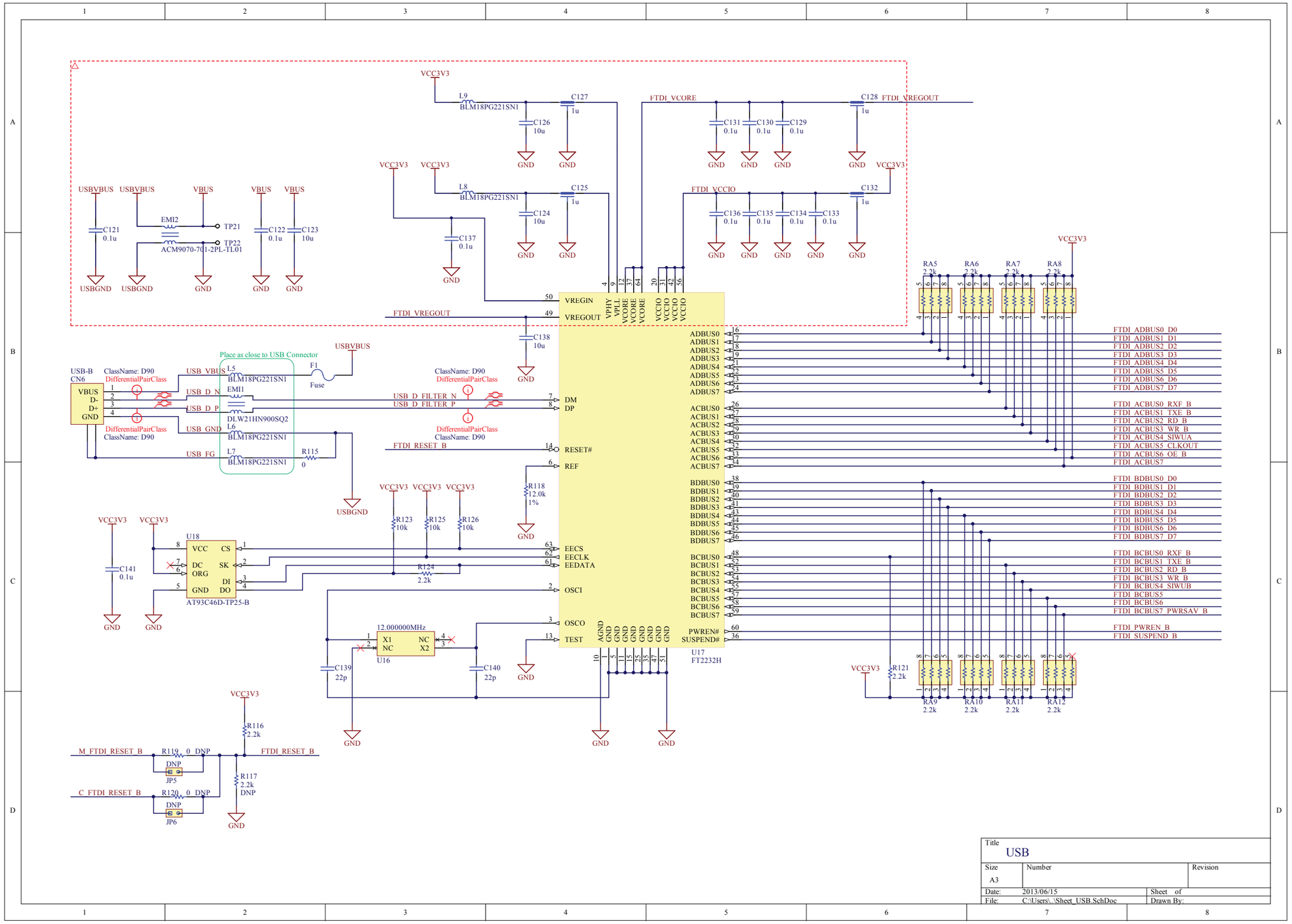


Figure 34 : Schematic – USB

4.3. Parts List

Table 48 : SAKURA-G Parts List

Description	Part Number	Maker	Designator	Spec.
Capacitor	UUD1C221MCL1GS	Nichicon	C1	220u
Capacitor	GRM188B31H104KA	Murata	C2	0.1u
Capacitor	C3216JB1C106KT	TDK	C3	10u
Capacitor	C2012X7R1E104K/0.85	Murata	C4, C17	0.1u
Capacitor	C1608X5R0J106MT	TDK	C5, C16, C18, C19, C22, C26, C30, C31, C34, C37, C78, C114, C123, C124, C126, C138	10u
Capacitor	PCJ0J391MCL1GS	Nichicon	C6, C21	390u
Capacitor	GRM188R60J475ME19D	Murata	C7, C9, C10, C12, C13, C15, C43, C44, C56, C60, C66, C70, C89, C94, C95, C96, C100, C103, C106, C109	4.7u
Capacitor	GRM32ER60J107ME20L	Murata	C20, C24, C42, C55, C59, C65, C69, C88, C99, C102, C105, C108	100u
Capacitor	NFM18PC105R0J3	Murata	C23, C79, C115, C125, C127, C128, C132	1u
Capacitor	C1005X7R1E104M (7)	Murata	C25, C27, C29, C33, C36, C38, C39, C40, C82, C85, C86, C118, C121, C122, C129, C130, C131, C133, C134, C135, C136, C137, C141	0.1u
Capacitor	GRM1555C1H102JA	Murata	C28, C32, C35	1000p
Capacitor	C1005X5R1A474K	TDK	C45, C46, C47, C48, C57, C58, C61, C62, C63, C64, C67, C68, C71, C72, C73, C74, C90, C91, C97, C98, C101, C104, C107, C110	0.47u
Capacitor	C1005JB0J105KT	TDK	C75, C76, C77, C111, C112, C113	1u
Capacitor	GRM155B11E103K	Murata	C80, C116	0.01u

Capacitor	GRM1555C1H220J	Murata	C139, C140	22p
Connector	B2P-VH(LF)(SN)	JST	CN1	
Connector	87832-1420	Molex	CN2, CN4	
Header	2131D2*20GSE	Linkman	CN3, CN5	
Connector	61729-0011BLF	FCI	CN6	
Diode	MMBD1501A	Fairchild	D1	
EMI Filter	DLW21HN900SQ2	Murata	EMI1	
EMI Filter	ACM9070-701-2PL-TL01	TDK	EMI2	
Fuse	MICROSMD050F-2	TE	F1	
SMA Jack	5-1814832-1	TE	J1, J2, J3, J4, J5, J6, J7	
Header	68001-202HLF	FCI	JP2	
Inductor	BLM18PG221SN1	Murata	L1, L2, L3, L4, L5, L6, L7, L8, L9	
LED	SML-310MTT86	Rohm	LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11, LED12, LED13, LED14, LED15, LED16, LED17, LED18, LED19, LED20, LED21, LED22, LED23, LED24, LED25, LED26, LED27	
Resistor	KRL3264-C-R010-F-T1	Susumu	R1	10m
Resistor	ERJ-6ENF6652V	Panasonic	R2	66.5k
Resistor	RK73B1ETTP561J	KOA	R3	560
Resistor	RK73H1ETTP7502F	KOA	R4	75k
Resistor	RK73H1ETTP3902F	KOA	R5	39k
Resistor	RK73H1ETTP5102F	KOA	R6	51k
Resistor	RK73H1ETTP1002F	KOA	R7	10k
Resistor	RK73H1ETTP1603F	KOA	R8	160k
Resistor	RK73H1ETTP2702F	KOA	R9	27k
Resistor	ERJ-6ENF1002V	Panasonic	R10	10k
Resistor	RK73B1ETTP102J	KOA	R11, R39, R41, R43, R47, R72, R73, R77, R93, R94, R95	1k
Resistor	RL1220S-1R0-F	Susumu	R12	1
Resistor	RK73Z1JTTD	KOA	R13, R14, R16, R46, R90	0

Resistor	RK73H1ETTP1R00F	KOA	R15	1
Resistor	ERJ2RKF61R9X	Panasonic	R17	61.9
Resistor	ERJ-2RKF4020X	Panasonic	R18, R19	402
Resistor	ERJ-2RKF8060X	Panasonic	R20	806
Resistor	ERJ2RKF40R2X	Panasonic	R21	40.2
Resistor	ERJ-2RKF3570X	Panasonic	R22	357
Resistor	ERJ2RKF49R9X	Panasonic	R23	49.9
Resistor	ERJ-2RKF27R0X	Panasonic	R24, R64	27
Resistor	RK73B1ETTP331J	KOA	R25, R26, R27, R31, R32, R38, R60, R65, R66, R71, R111	330
Resistor	RK73B1ETTP103J	KOA	R28, R29, R30, R33, R34, R36, R58, R59, R63, R67, R68, R70, R109, R110, R114, R123, R125, R126	10k
Resistor	RK73Z1ETTP	KOA	R37, R40, R62, R113	0
Resistor	RK73B1ETTP101J	KOA	R42, R74	100
Resistor	RK73B1ETTP151J	KOA	R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R99, R100, R101, R102, R103, R104, R105, R106, R107, R108	150
Resistor	RK73B1ETTP222J	KOA	R61, R112, R116, R121, R124	2.2k
Resistor	RK73H1JTTD1000F	KOA	R75, R76, R91, R92	100
Resistor	RK73B1JTTD101J	KOA	R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R96, R97, R98	100
Resistor	MCR18EZPJ000	Rohm	R115	0
Resistor	RK73H1ETTP1202F	KOA	R118	12.0k
Resistor Array	MNR04M0APJ103	Rohm	RA1, RA2, RA3, RA4	10k
Resistor Array	MNR04M0APJ222	Rohm	RA5, RA6, RA7, RA8, RA9, RA10, RA11, RA12	2.2k
SPDT Switch	MS-13AAP1	Nikkai	SW1	
Switch	CHS-04TB1	Copal	SW2	

		Electronics		
Switch	B3FS-1000P	Omron	SW3, SW4, SW6, SW7, SW8, SW9, SW11, SW12	
Switch	CHS-08TB1	Copal Electronics	SW5, SW10	
Test Pin	RCTCTE	KOA	TP15, TP16, TP19, TP20	
FPGA	XC6SLX75-2CSG484C	Xilinx	U1	
FPGA	XC6SLX9-2CSG225C	Xilinx	U2	
Regulator	LT3083EQ#PBF	LT	U3, U7	
Regulator	MCP1726-ADJE/MF	Microchip	U4, U5, U6	
Amplifier	AD8000YRDZ	ADI	U8	
Logic IC	74LVC157APW,118	NXP	U9	
SPI Flash Memory	AT45DB321D-SU	Adesto	U10, U13	
Oscillator	ECS-3525-480-B-TR	ECS	U11, U14	48MHz
Supervisor IC	STM6779YWB6F	STMicro	U12, U15	
Crystal Unit	CX3225GB12000D0HEQZ1	AVX	U16	12MHz
USB I/F IC	FT2232HL-REEL	FTDI	U17	
SPI EEPROM	AT93C46D-TH-B	Atmel	U18	
Variable Resistor	ST32ETA203	Copal Electronics	VR1	20k

4.4. Board Layout

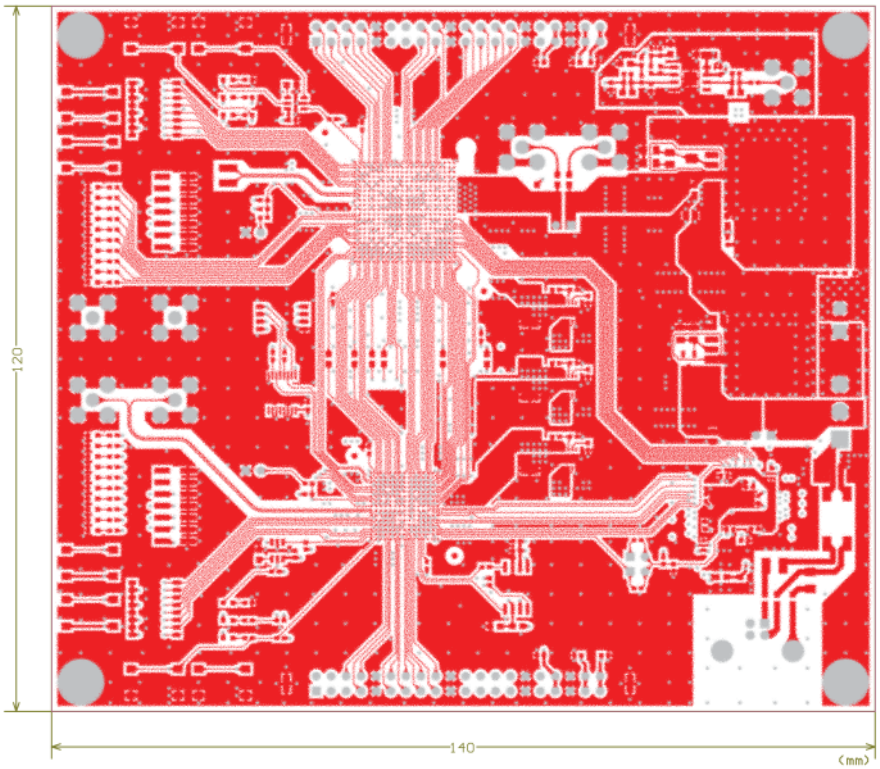


Figure 35 : L1 Pattern

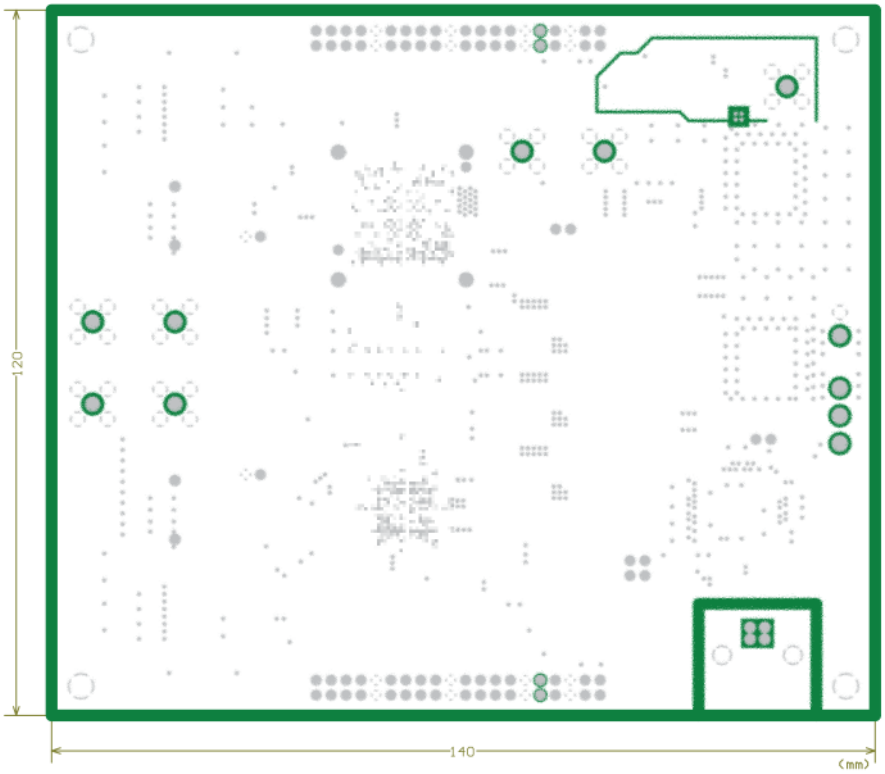


Figure 36 : L2 Cut Pattern

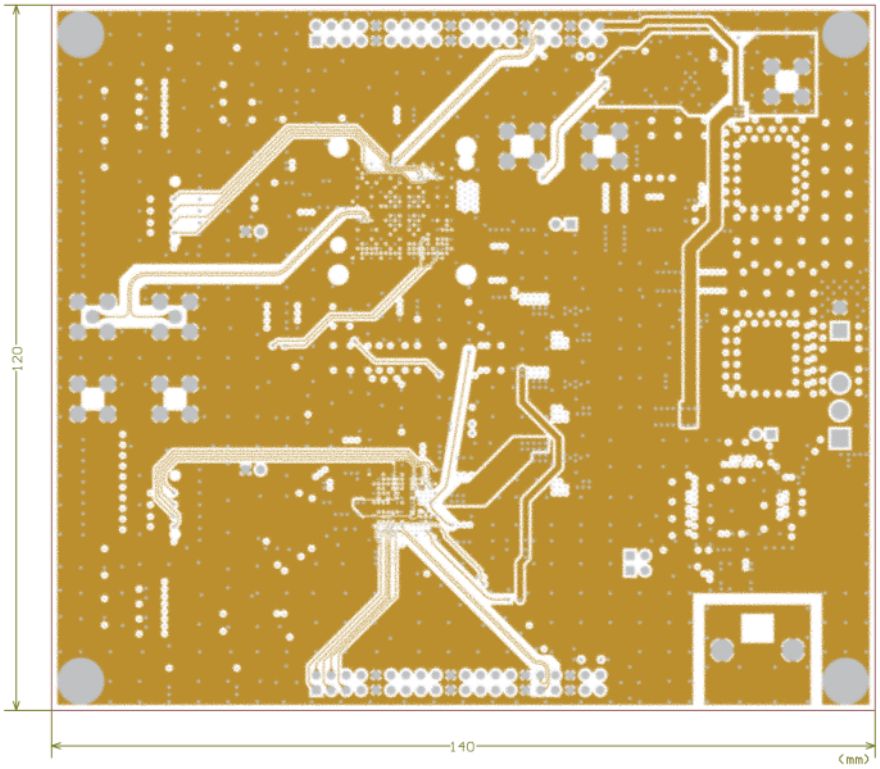


Figure 37 : L3 Pattern

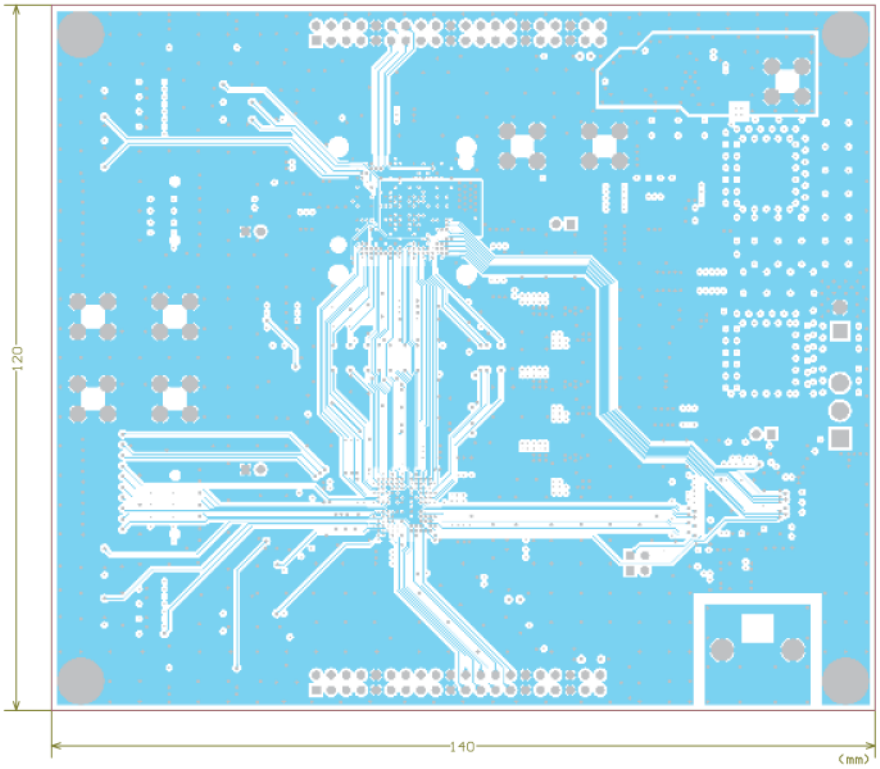


Figure 38 : L4 Pattern

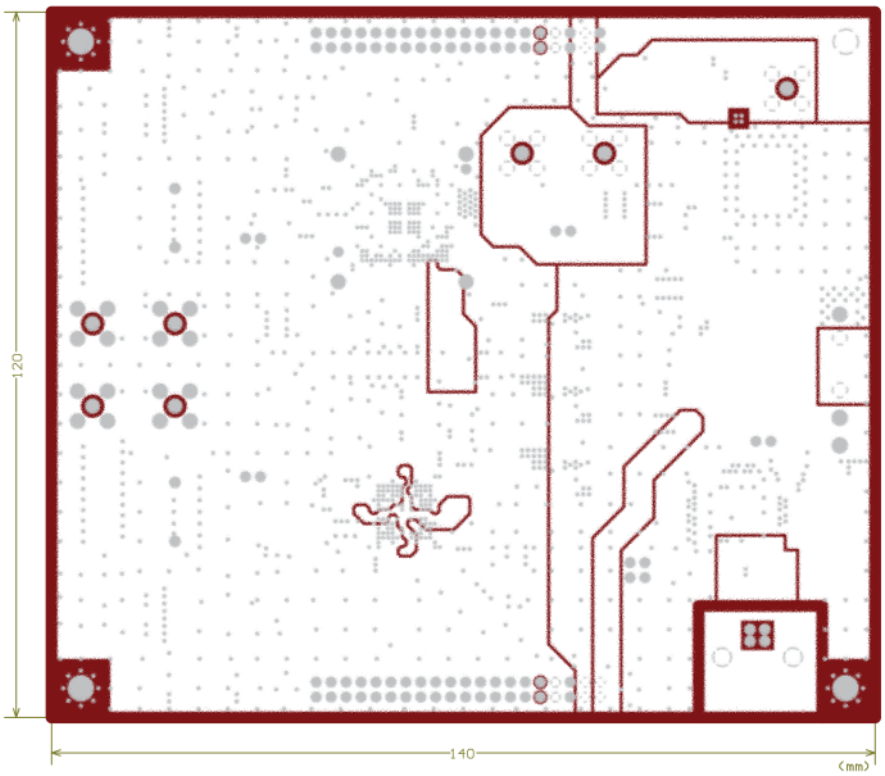


Figure 39 : L5 Cut Pattern

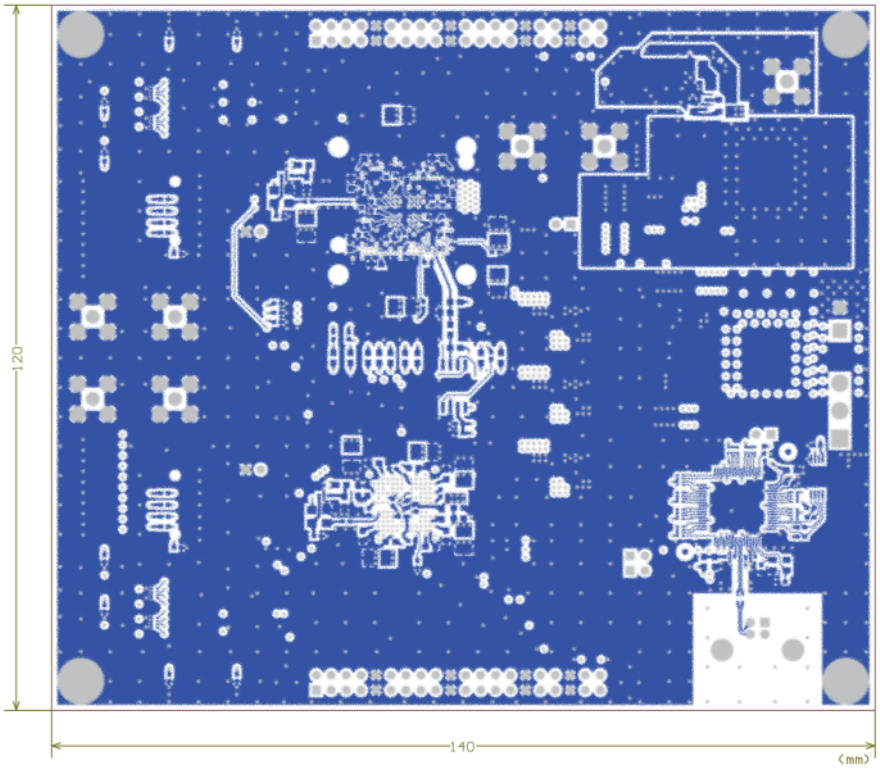


Figure 40 : L6 Pattern

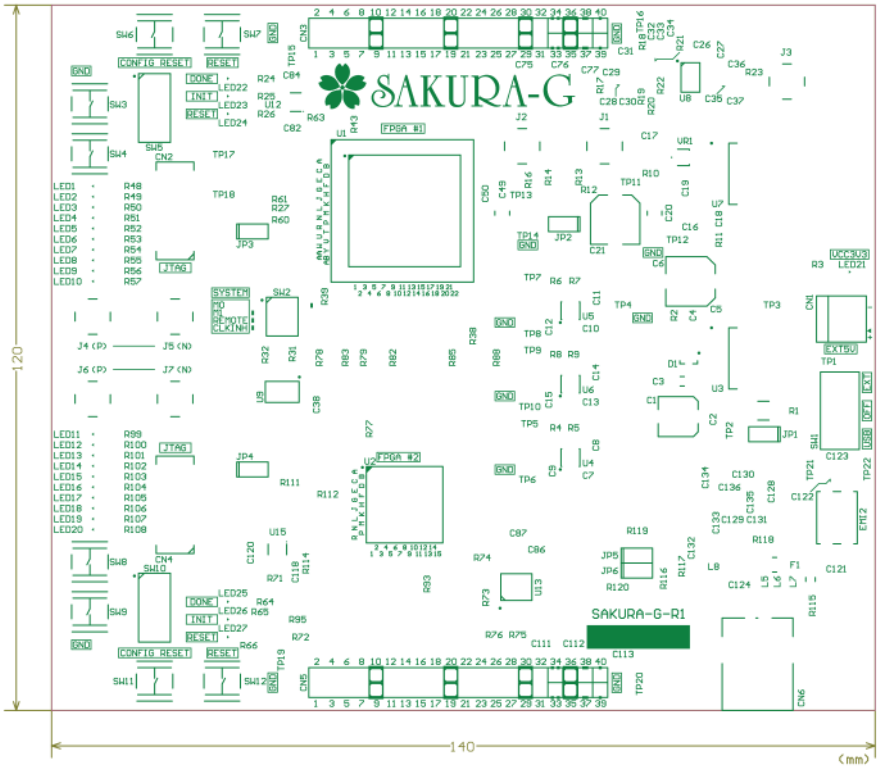


Figure 41 : Top Silk

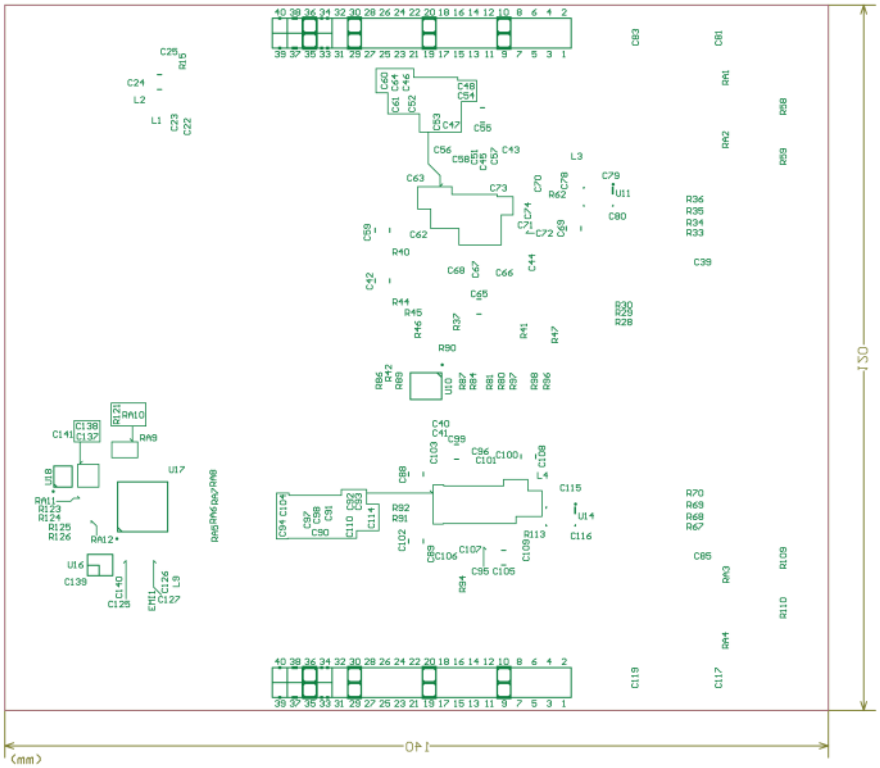


Figure 42 : Bottom Silk (flipped)

Please ask to sales for detail of board layout.

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