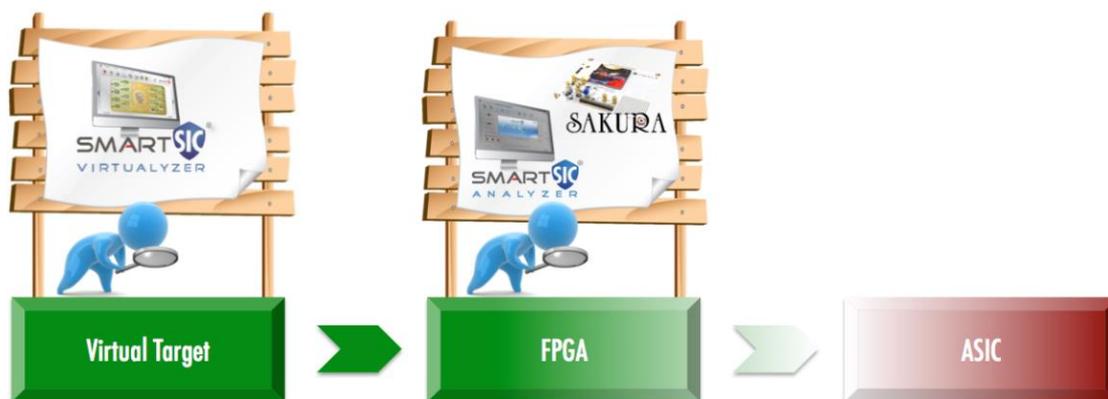


## Secure-IC and MTM-Systems partner for standard security evaluation test platforms

*MTM-Systems and Secure-IC share the common vision of testing electronic designs against non-invasive attacks straight at the source code, as early as possible in the design flow.*

As one might know, systems on chip are usually designed then tested against threats at the ASIC level. When a design is not securely certified, getting back to a new design is synonymous with wasting time and money. Nowadays key technologies to ease security testing are Virtual Prototyping and Emulation in FPGA, which consist in analyzing a design before it is mapped into an ASIC.

The partnership between Secure-IC and MTM-Systems aims at giving designers an easier access to the new ways of anticipating the security weaknesses of their systems. **Virtual Prototyping** consists in detecting security issues straight from the source code and has been made easier by Secure-IC's **Smart-SIC Virtualyzer**. On another hand, **Emulation in FPGA**, allowing real-time testing, has been permitted by MTM's **SAKURA Boards**, coupled with Secure-IC's **Smart-SIC Analyzer**.



From virtual to emulation, MTM & Secure-IC realize seamless non-regression testing throughout the design flow of a product.

Charles Thooris, the APAC Sales and Marketing Manager for Secure-IC, does not hide his enthusiasm for such a partnership. "We have been using MTM's SAKURA Boards with our Analyzers for more than one year, with a great satisfaction", he says. "It's always been a pleasure to partner with them and I believe and hope it will go on in the foreseeable future."

"We are delighted to work with Secure-IC to deliver our hardware coupled with their sophisticated software", Akashi Satoh, leader of SAKURA project for MTM Systems, says. "Physical security analysis in design phase before production was achieved by this collaboration while conventional tools evaluate existing hardware."

These tools have the advantage to detect security flaws early and supply consistent security policy verification throughout the design cycle. By permitting an earlier analysis and a better anticipation of the security loopholes, both MTM-Systems and Secure-IC strongly believe that their association will be seen by designers as a pleasant opportunity to improve their products and to meet tomorrow's requirements.

**Secure-IC will be exhibiting the Smart-SIC Virtualyzer and Smart-SIC Analyzer with SAKURA board at CARTES in Paris on the 4<sup>th</sup>, 5<sup>th</sup>, 6<sup>th</sup> November!**

**About MTM-Systems:**

*Univ. Electro-Communications (UEC) and Morita Tech started the SAKURA hardware security project as the successor of the SASEBO Project. In the project, various experimental hardware and software were developed to contribute to the research on physical security analysis of cryptographic modules. MTM-Systems, founded with the support from UEC, delivers the SAKURA products and UEC provides technical information about SAKURA.*

*Please visit: <http://shop.mtmsystems.jp/>*

**MTM-Systems Contact:**

Mr Shirono (CEO), Email: [shirono@mtmsystems.jp](mailto:shirono@mtmsystems.jp)

**About Secure-IC:**

*Secure-IC, the Trusted Computing Company, develops trusted computing security technologies for embedded systems to protect them from malevolent attacks and cyber threats. Working with top scientists in the field, Secure-IC is a thought leader in the cyber security domain with best-of-breed technologies that assess the vulnerability of any embedded system and IP-cores that protect hardware products from state-of-the-art attacks. The company serves the market from three different locations: France for Europe, Singapore for Asia Pacific and the Silicon Valley for North America.*

*Please visit: <http://www.secure-ic.com>*

**Secure-IC Contact:**

Charles Thooris, Tel.: +65-8427-6835, Email: [charles.thooris@secure-ic.com](mailto:charles.thooris@secure-ic.com)